Application Note AN-10

XR-C262 High-Performance PCM Repeater IC

INTRODUCTION

The XR-C262 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of $-40^{\circ}C$ to $+85^{\circ}C$. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Built-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The XR-C-262 operates with a single 6.8-volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock-extractor section of XR-C-262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to "off" state automatically when there is no input signal present. Compared to conventional repeater designs using discrete components, the XR-C262 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

This application note outlines the basic design principles and the electrical characteristics of the XR-C262 monolithic repeater IC. In addition, circuit connections and applications information are provided for its utilization in T-1 type 1.544 Megabit PCM repeater systems.

FUNDAMENTALS OF PCM REPEATERS

The Pulse-Code Modulation (PCM) telephone systems are designed to provide a transmission capability for multiple-channel two-way voice frequency signals which are transmitted in a digital PCM format. In order to minimize error rates, and provide transmission over long distances, this digital signal must be regenerated at periodic intervals, using a regenerative repeater system. Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator.

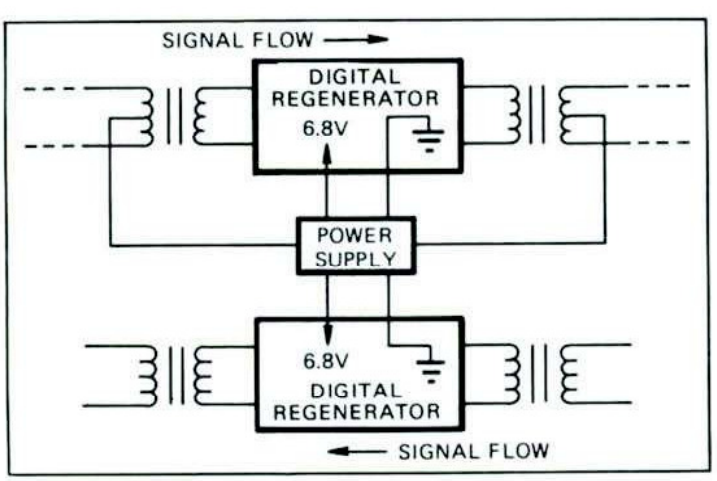

Figure 1. Block Diagram of a Bi-Directional Repeater System.

In the United States, the most widely used PCM telephone system is the T-1 type system which operates at a data rate of 1.544 Mbps, with bipolar data pulses. It can operate on either pulp- or polyethylene-insulated paired cable that is either pole-mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772 kHz is less than 36 dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The T-1 type transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end cross-talk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The XR-C262 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C262 ICs, one for each direction of information flow.

OPERATION OF THE XR-C262

The XR-C262 monolithic repeater is packaged in a 16-pin dual-in-line hermetic package, and is fabricated using bipolar process technology. The functions of the circuit terminals are defined in Figure 2, in terms of the monolithic IC package.

A more detailed system block diagram for the monolithic repeater system is given in Figure 3. The system blocks shown within the dotted area are included on the monolithic chip. The numbers on the circuit terminals correspond to the pin numbers of the 16-pin IC package containing the repeater chip. In terms of the system block diagram of Figure 3, the overall repeater operation can be briefly explained as follows.

The bipolar PCM signals which are attenuated and distorted due to the preceding transmission medium are applied to the input of a preamplifier (Block 1) through an Automatic Line Build-Out (ALBO) circuit. The impedance, Z_1, corresponds to the passive section of the ALBO network. The preamplifier section, along with the passive equalizer networks Z_2 and Z_3 connected in feedback around it, provides gain to compensate for line losses and band-limiting to reject unwanted noise as well as gain and phase equalization to shape received pulses.

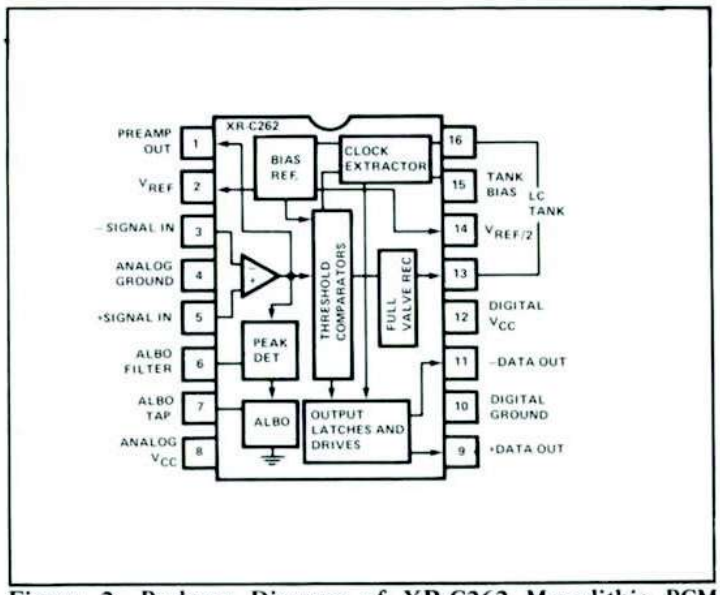

Figure 2. Package Diagram of XR-C262 Monolithic PCM Repeater.

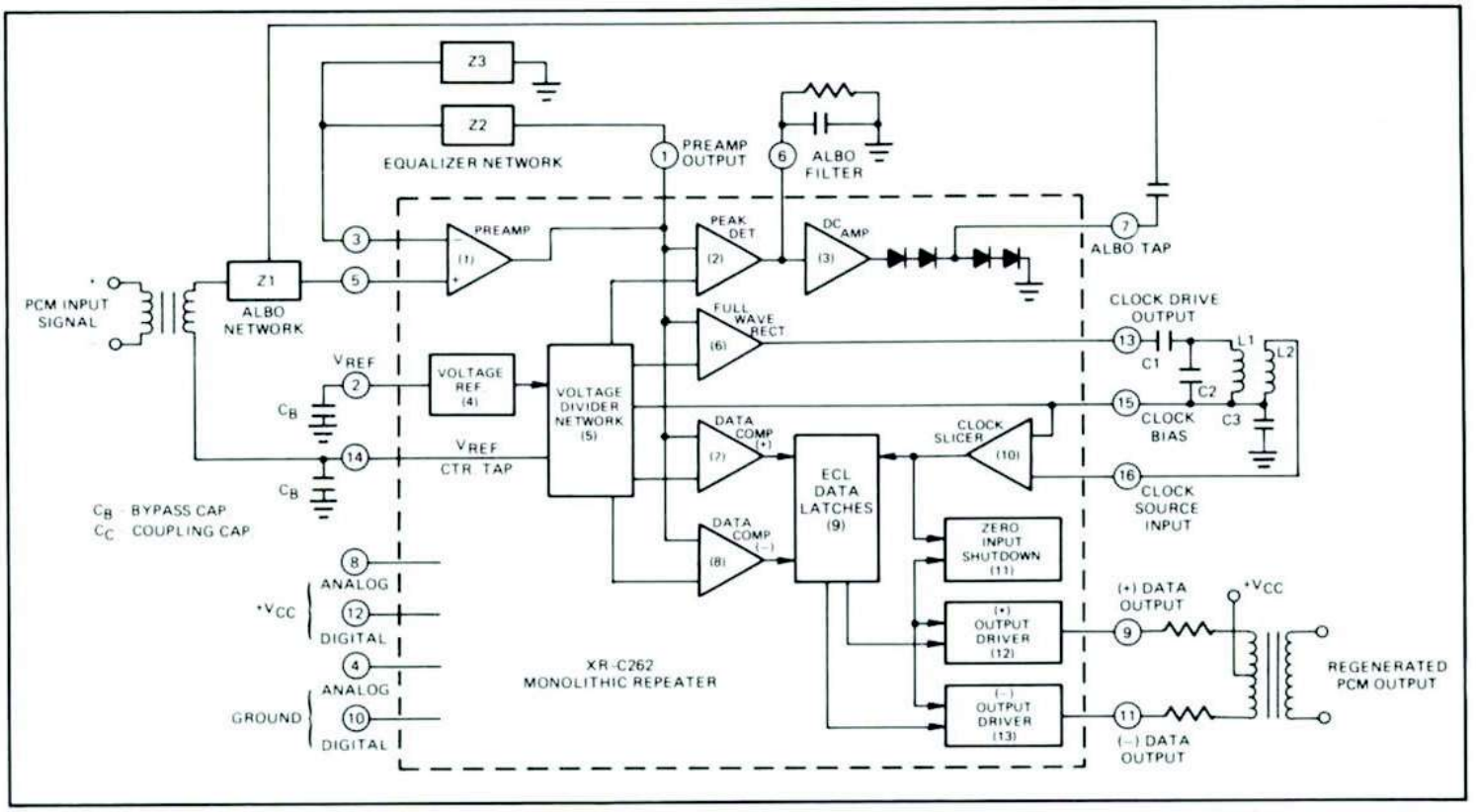

Figure 3. Detailed Block Diagram of the XR-C262 Monolithic Repeater System.

The ALBO circuitry provides attenuation and shaping to automatically adjust for varying cable characteristics. The output of the preamplifier is controlled to swing between two established peak levels. This is accomplished by feedback circuitry, and is similar in concept to automatic gain control. When the preamplifier output passes through the peak thresholds it is detected by the peak detector (Block 2) and produces a signal which is used to control a feedback loop establishing the attenuation and shaping of the ALBO network. The actual circuit design associated with this function is described in more detail in the discussion of peak detection and ALBO circuitry.

The output of the preamplifier drives a set of data comparators which are internally biased from a voltage reference (Block 4) and the precision voltage divider network (Block 5). Thus, the preamplifier output is "sliced" at various voltage levels to eliminate the effects of the baseline noise. This output is full-wave rectified and amplified through Block 6 of Figure 3. The resulting signal has a strong Fourier component at the clock frequency and is used to drive a high Q ($\approx$100) resonant circuit tuned to that frequency. The output of the resonant circuit is transformer-coupled to a zero-crossing detector and clock limiter (Block 10). The resultant output is the desired recovered timing. This resonant circuit is driven by a low impedance amplifier, and the resulting clock edges are in phase with the peak of the received pulses.

The regeneration of the data is achieved through the two data comparators (Blocks 7 and 8) and the ECL latches (Block 9) which function as tracking flip-flops. The positive and negative data paths are separate; and, with the exception of the data limiter and slicer levels, identical in design. The preamplifier output is sliced at about 45 percent of the peak voltage and its amplitude is limited to provide digital data pulses. The data is applied to one of the inputs to the tracking flip-flop, whose state is latched and unlatched by the clock. During acquisition, the flip-flop acquires data; during hold, further data transitions are ignored and the state of the flip-flop output determines whether an output pulse is transmitted. The implication of using the clock to perform data sampling is that path delays of the data and clock must be controlled to be equal. The monolithic integrated circuit technology affords this control. The advantage of this technique is that the need for clock shifting or strobe pulse generating circuitry for accurate sampling alignment is eliminated. Actual circuit implementation resulted in a 40 nsec misalignment of clock and data. This 40-nsec error in sampling time amounts to less than .4 dB degradation in SNR performance. Figure 4 shows the idealized timing and signal waveforms within the circuit.

The output drivers use latched data and clock to produce an output pulse-width which is accurately controlled by the duration of the clock. Non-saturating output drivers (Blocks 12 and 13) insure that output pulse rise and fall times are less than 100 nsec. The zero input shut-down circuitry (Block 11) guarantees that in the event incoming data disappears, the output switches will not latch in the "on" state. When no input signal is present, the absence of clock is sensed and the output drivers are held in the "off" state.

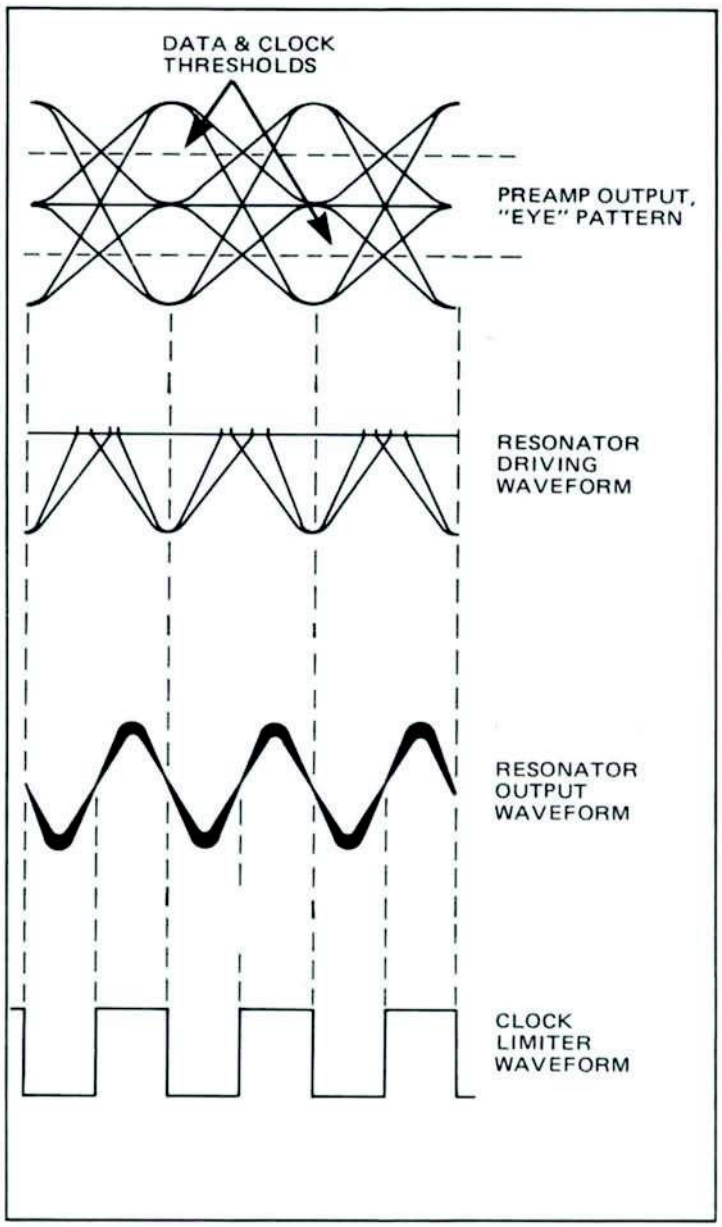

Figure 4. Timing Diagrams of Voltage Waveforms within the Clock Regeneration Section.

Figure 5 shows a practical circuit connection for the XR-C262 in an actual PCM repeater application for 1.544 Mbps T-1 repeater system. For simplification purposes, the lightening protection circuitry and the second repeater section for the reverse channel are not shown in the figure.

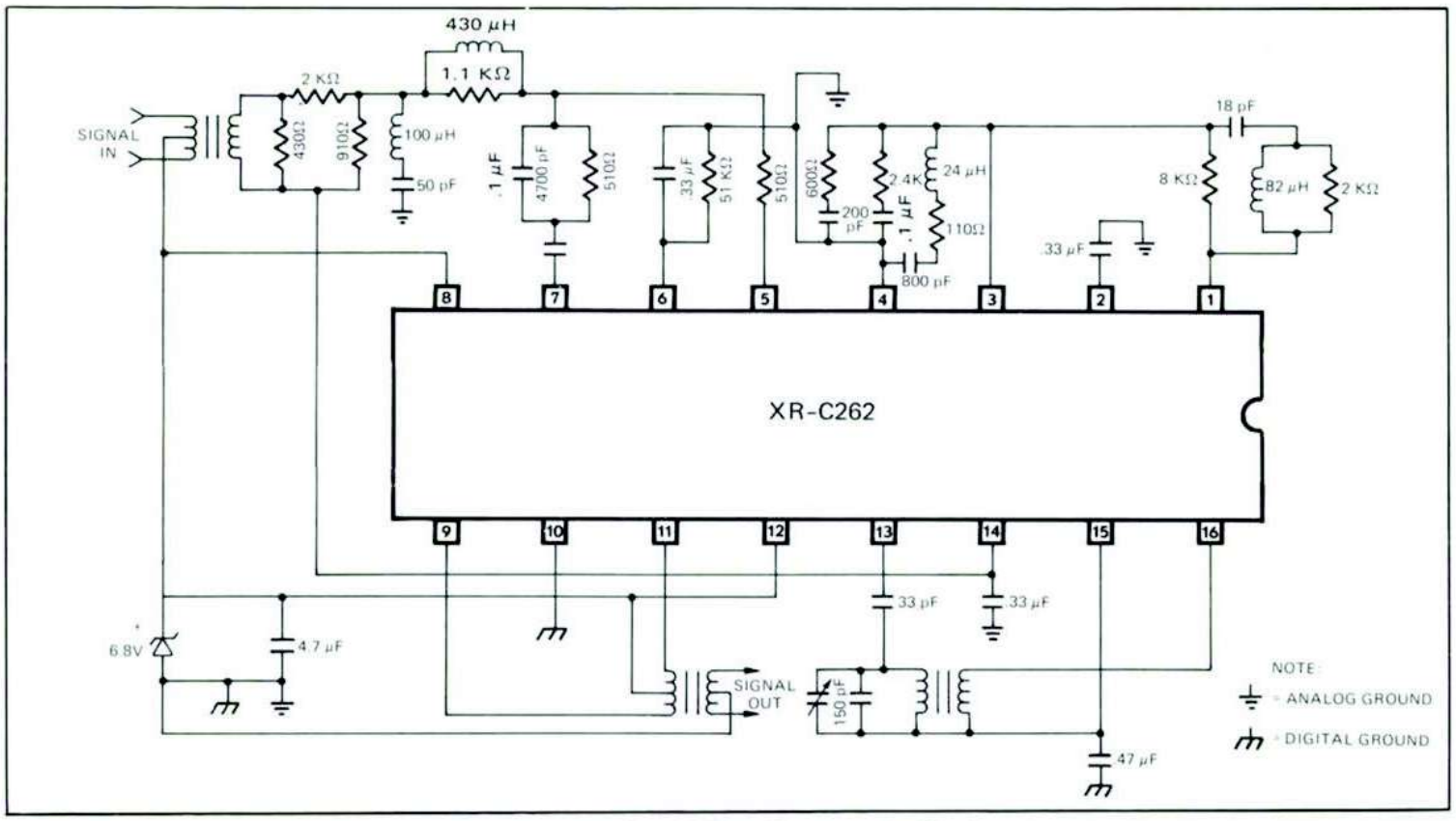

Figure 5. A Recommended Circuit Connection Diagram for T-1 Type Repeater Application.

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Figure 6):

The circuit diagram of the preamplifier section is shown in Figure 6. This section is designed as a single-stage high-gain amplifier with differential inputs and a single-ended output. The amplifier output is internally connected to the peak-detector, full-wave rectifier and the data-comparator sections. The circuit exhibits a high differential input resistance ($\approx 10^6$ ohms) and a low output impedance ($\approx$ 80 ohms). It has a nominal voltage gain of 69 dB at DC and $\geq$ 50 dB at 1 MHz. The frequency response of the circuit exhibits a single-pole roll-off characteristics.

Peak-Detector and ALBO Section (Figure 7):

The peak-detector circuit is designed to detect the peaks of the preamplifier output, provided that these peaks exceed the internal detection threshold levels. This peak information is then low-pass filtered and is used to control the current in a diode string which acts as a variable-loss or "variolosser" element in a feedback path. In the circuit, the comparators conduct whenever the preamp output exceeds the (+) threshold in a positive direction or the (−) threshold in a negative direction. Transistor Q_5 then injects a pulse of current into the ALBO filter. In the steady state, DC level across the ALBO filter controls the current through the diode string; and the dynamic resistance of the diodes acts as the variolosser element. The usable linear resistance range in this application is almost three orders of magnitude ranging from 11Ω to $\approx$ 6 KΩ.

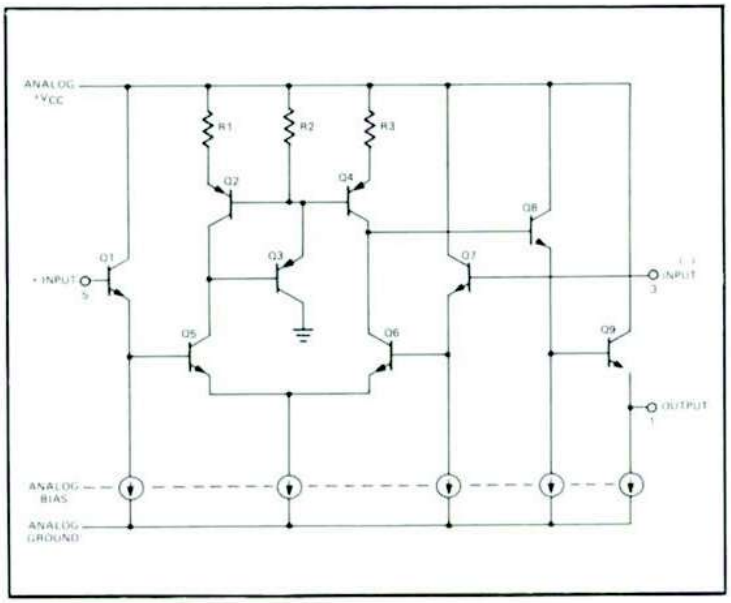

Figure 6. Circuit Diagram of Preamplifier Section.

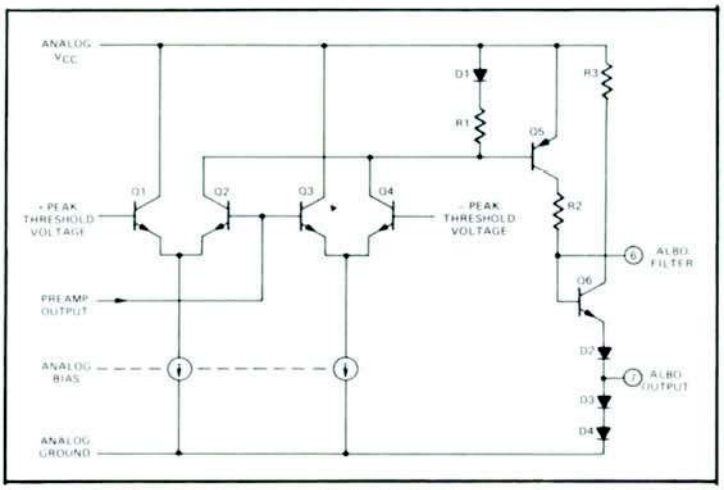

Figure 7. Circuit Diagram of the Peak-Detector and the ALBO Sections.

Data Latches (Figure 8):

The data latches are required to be impervious to data transitions in the latch mode, and to be "transparent," (i.e., tracking the input data) during the tracking mode. Figure 8 shows the basic circuit configuration used in the XR-C262, which meets the above-mentioned performance requirements. During the time when the clock pulse is high, the acquisition transistors Q_1 and Q_2 are differentially switched with data transitions, and the data is coupled to the respective bases of Q_3 and Q_4. When the clock pulse goes low at the sample time (see Figure 4), the information is regeneratively latched into Q_3 and Q_4. While the clock is low, further data transitions have no effect upon the state of the flip-flop. A more detailed description of the timing waveforms is given in Figure 13.

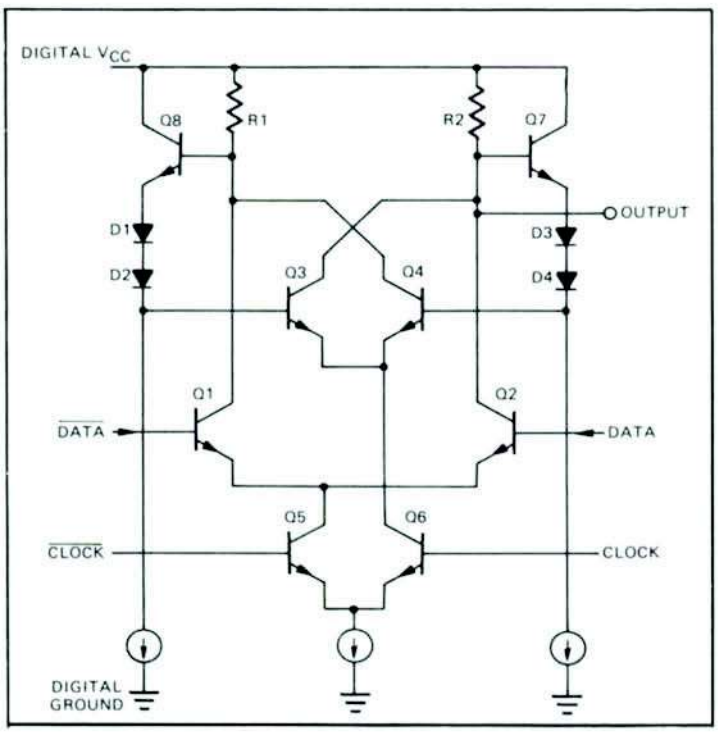

Figure 8. Circuit Configuration for Tracking Data Latches.

Threshold Circuitry (Figure 9):

Threshold circuitry is a low impedance voltage-divider circuit corresponding to Block 5 of Figure 3, and it establishes the fixed levels required for data, clock and peak detection. It is important that the thresholds are insensitive to temperature variations, and that they are of sufficiently low impedance to guarantee that there is no threshold variation due to changing signal conditions. The reference voltages of the peak-detector, data, and clock thresholds are set by a resistor chain which divides down the voltage of the on-chip zener diode. The ratios of data threshold to peak-detector threshold and that of clock threshold to peak-detector threshold are both set at 45 percent. In the actual circuit implementation, as shown in Figure 10, a compound connection of PNP's and NPN's are used to reduce the output impedance of the reference levels. The currents through the NPN and PNP transistor strings are set so as to insure that the base emitter voltage drops of the NPN's and PNP's are nominally the same. The output impedance of the resulting reference voltage taps are about 300 ohms. The center tap of the buffered divider is brought to a separate package terminal (Pin 14 of Figure 3) for biasing the preamplifier input.

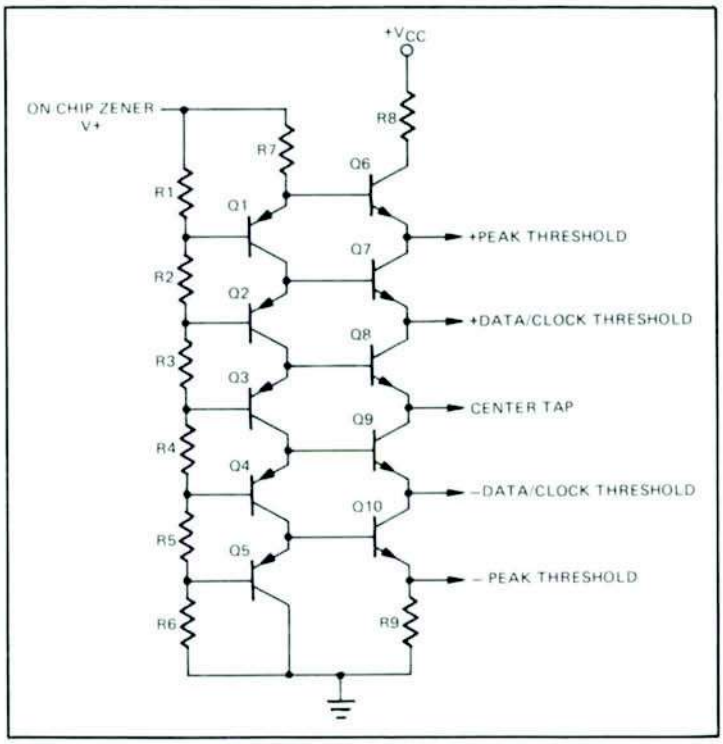

Figure 9. Internal Voltage-Divider Network for Comparator Threshold Setting.

Clock Recovery Section (Figure 10):

Clock recovery circuitry consists of a full-wave rectifier, an external L-C resonant circuit, a zero crossing detector, and limiting amplifier, as shown in Figure 10. The full-wave rectifier circuit, comprising of cross-coupled transistor pairs Q_1 through Q_4 has a net voltage gain of 2, which is obtained by Setting $R_1 = R_2 = (1/2)R_3$. The rectified output is then buffered by the Darlington emitter-follower stage made up of Q_5 and Q_6, and applied to the external L-C resonant circuit.

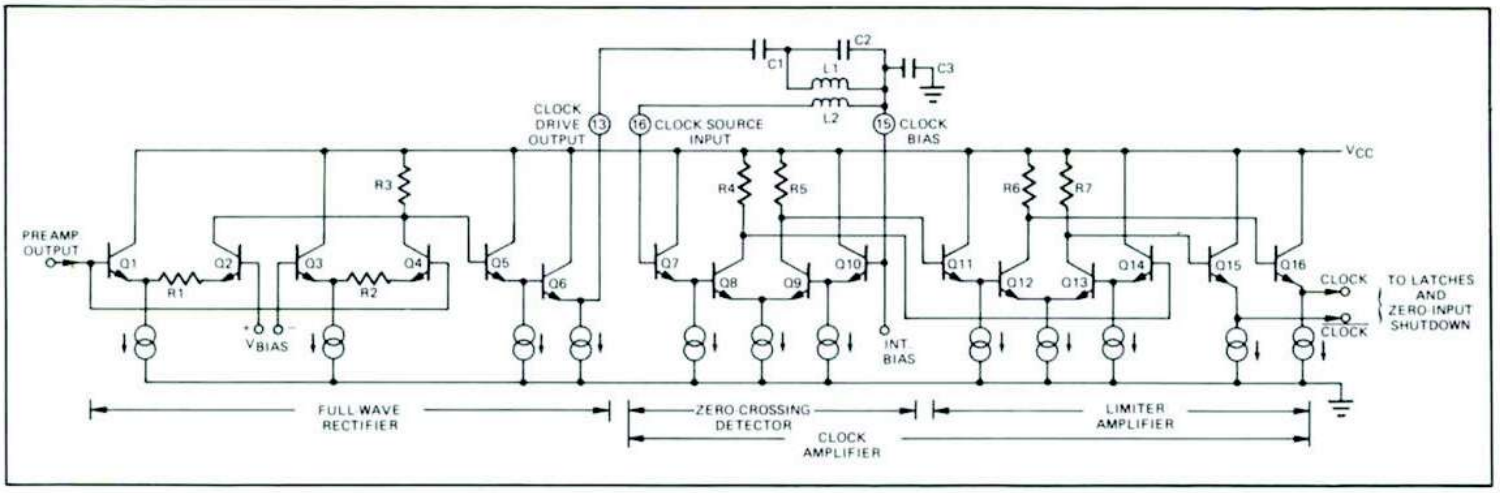

Figure 10. Circuit Diagram of the Clock Recovery Section.

Q_6 is operated at a high bias current level to provide an output impedance of less than 15Ω. This low impedance is required to insure that the L-C tank-drive circuitry looks like a voltage source.

The inductor of the resonant tank circuit is also a transformer which couples the sine wave signal to the zero crossing detector and limiting amplifier. The zero crossing detector is a differential amplifier with a nominal voltage gain of 20 and input impedance of 4 MΩ. The sine wave from the resonant circuit is sliced to produce a square wave with sharp transitions at the zero crossings. This eliminates timing variations that may be caused by amplitude changes of the sine wave signal. The output of the zero crossing detector is further enhanced by the limiter which is another differential pair with a nominal voltage gain of 30. The output of this amplifier is a 1.5V peak-to-peak square wave clock which drives the data latches and the output drivers.

Zero-Input Protection Circuit (Figure 11):

The zero input protection circuitry accomplishes the dual task of preventing the output switches from latching in an "on" state, as well as reducing the likelihood of output pulses with no input signal. The data, clock, and regenerator circuitry are all balanced DC coupled circuits. Controlling the steady state, no-signal condition of these circuits without building an unacceptable offset into the path is not practical. Instead, a retriggerable one-shot that uses the saturation characteristics of PNP transistors is used to control the level of the clock into the output switches. This technique uses the bandpass characteristics of the timing recovery resonant circuit to reject out of band signals thus minimizing the chance of producing output pulses with no input signal and the presence of noise. Figure 11 shows the basic implementation of the zero-input protection circuit. Q_1 and Q_2 function as a simple retriggerable one-shot. The transistor Q_2 is a lateral PNP device with a limited frequency capability and long storage-time delay. The existence of the 1.544 MHz clock causes Q_2 to saturate and remain in saturation while clock pulses are present. The comparatively long time constant associated with Q_2 coming out of saturation ($\approx$ 5 μsec) insures that, when data is present, the zero input protection has no effect upon operation. When data disappears there is no clock to retrigger the one-shot, thus Q_2 comes out of saturation, causing Q_3 to saturate which pulls the respective clock lines high, and disables both output drivers in their "off" state.

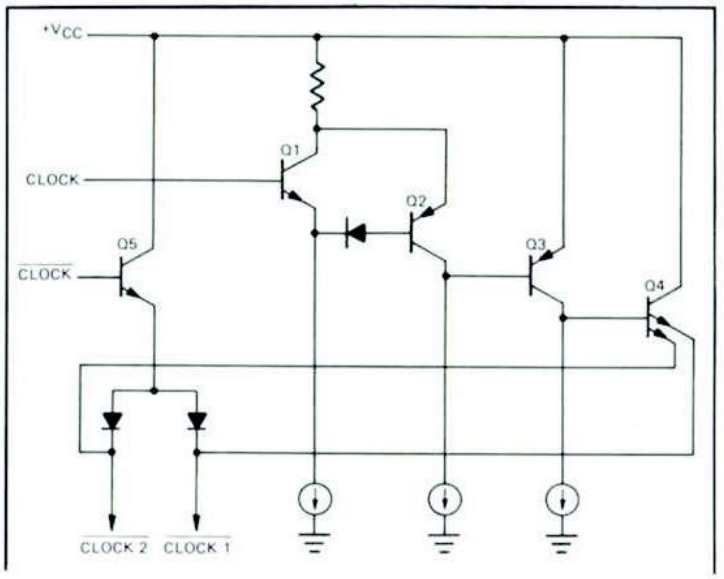

Figure 11. Zero-Input Shutdown Circuit for Output Protection.

Output Drive Circuitry (Figure 12):

The output drive circuitry is made up of two identical channels as indicated in the block diagram of Figure 2. The circuit configuration for each of these driver sections is shown in Figure 12. The output would follow the data input from the latches only when the clock input is at a "high" state, i.e., with Q_2 off and Q_3 on. In this manner, the output pulse-width is controlled by the clock. To provide the fast turn-on and turn-off of the output drivers, all the transistors operate in a nonsaturating state. Q_4 forms an active clamp to reduce voltage swing at the base of Q_6, and the clamp diode D_5 prevents the saturation of the output driver Q_7. Because of the biasing scheme mentioned above, the amplitude of the clock and the latched data are insensitive to supply voltage and temperature changes. Thus, the variations of the regenerated pulse-width over temperature and supply are minimized.

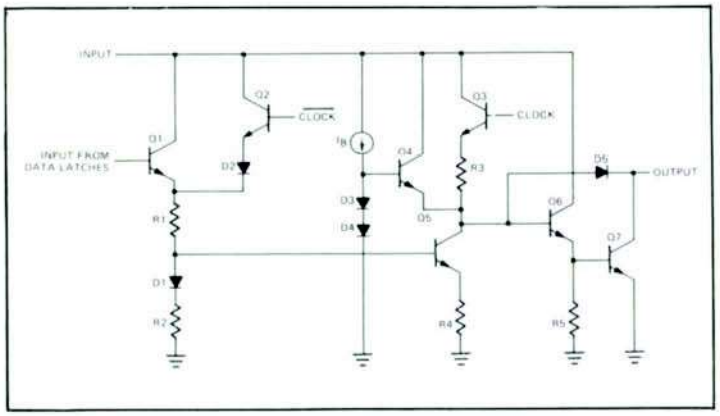

Figure 12. Circuit Configuration for the Output Drivers.

Timing Waveforms (Figure 13):

Figure 13 illustrates the relative time and phase relationships between the signal levels at various points within the circuit. For the purpose of illustration an input data pattern comprised of a string of "ONE"s is assumed, which looks like a nearly sinusoidal input, after having traveled through a dispersive transmission medium such as a long cable. Waveform (1) is the output of the preamplifier; waveforms (2) through (5) are the outputs of the two data comparators driven by the preamplifier output (see Figure 3). Waveform (6) is the low-level clock signal obtained from the resonant tank circuit, at pin 16 which is then amplified and "sliced" by the clock-recovery circuitry (see Figure 11) and appear as the internal clock signals shown as waveforms (7) and (8). The waveform (9) shows the output of one of the data latches (Figure 8) as a function of the clock and data inputs. The output of the latch tracks $\overline{+DATA}$ when the clock is low, and stays latched in that condition when the clock goes high. The output drive at pin 9, which is shown as waveform (10) will then go low only when the waveforms (8) and (9) are low. The waveform (11) shows the second output available at pin 11. These two outputs are then differentailly combined by the output transformer (see Figure 3) to provide the regenerated bipolar output pulses shown in waveform (12) of Figure 13.

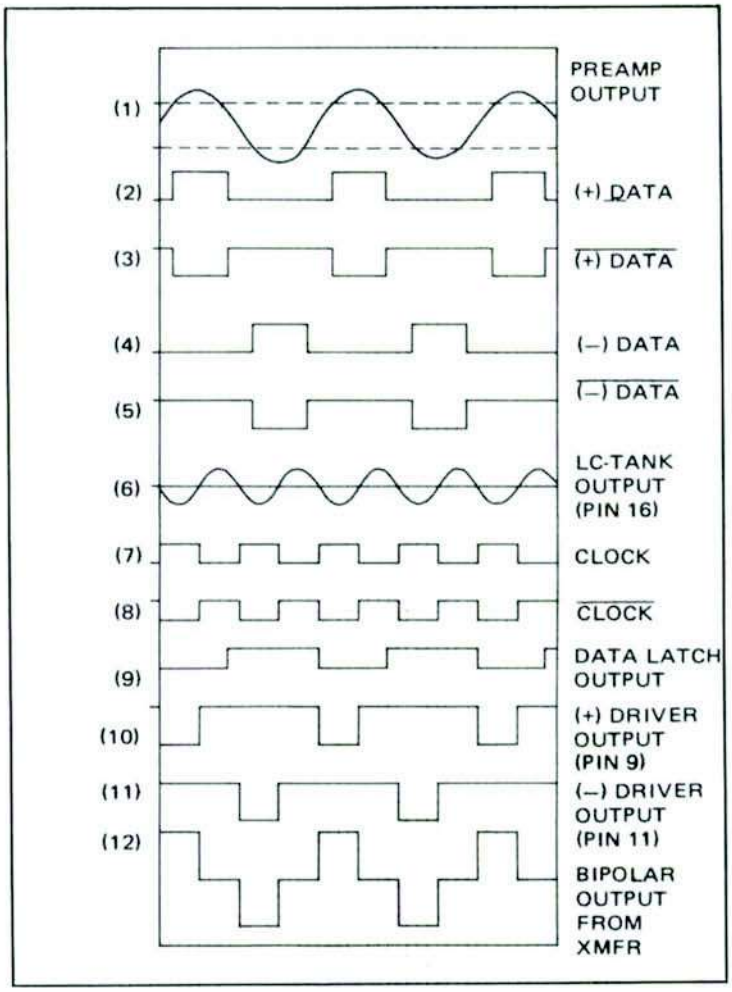

Figure 13. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern.

ELECTRICAL CHARACTERISTICS

$+V_{CC}$ = 6.8 Volts, T_A = −40°C to +85°C.

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	−15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
Comparator Thresholds					Measured at Pin 1 relative to Pin 14
ALBO Threshold	0.75	0.9	1.1	V	
Clock Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					Measured at Pins 9 and 11
Output High Swing	5.9	6.8		V	R_L = 400Ω
Output Low Swing	0.6	0.7	0.9	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	294	324	354	nsec	
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Storage Temperature Range	−65°C to +150°C

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-C262	CERDIP	−40°C to +85°C

PACKAGE INFORMATION