Application Note AN-04

XR-C277 Low-Voltage PCM Repeater IC

INTRODUCTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Mega bits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltages (6.3 volts and 4.4 volts) with a supply current of less than 13 mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

FUNDAMENTALS OF PCM REPEATERS

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator. The XR-C277 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C277 IC's, one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C277 monolithic IC.

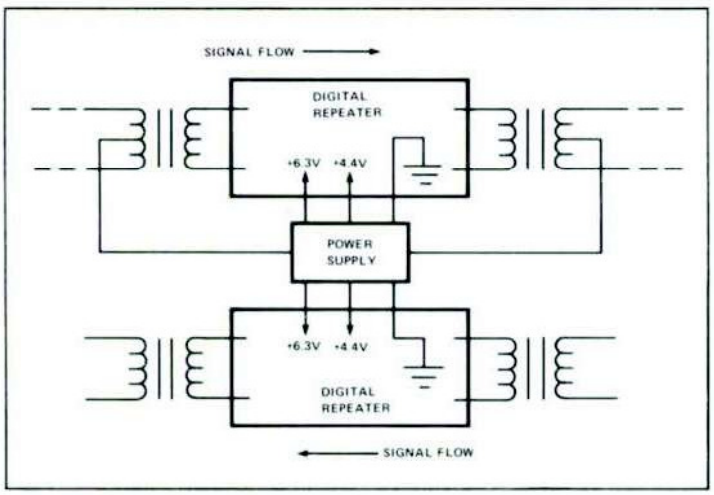

Figure 1. Block Diagram of a Bi-Directional Digital Repeater System

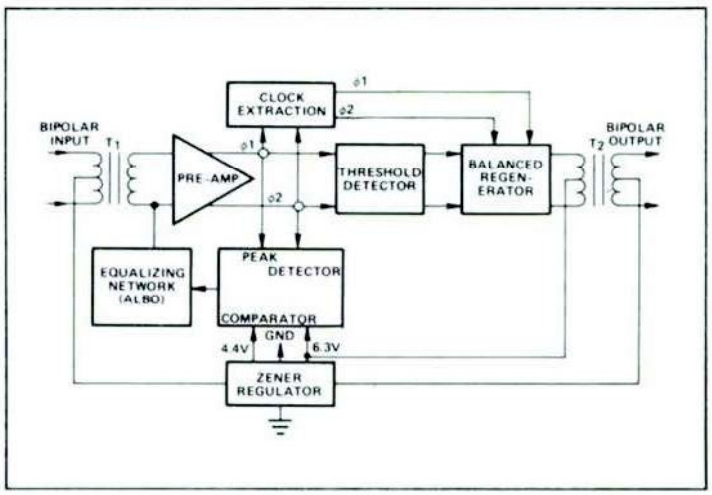

Figure 2. Functional Block Diagram of a Digital PCM Repeater System

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium, is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization and, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544 MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse is in turn applied to a discrete output transformer which is used to drive the next section of the paired cable.

Additional References on PCM Repeaters:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25-97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99-143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1-25.
4. Fultz, K. E. and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405-1452.
5. Tarbox, R.A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 – 46-10.

OPERATION OF THE XR-C277

The XR-C277 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line package.

The circuit is designed to operate with two positive supply voltages, V^{++} and V^{+} which are nominally set to be 6.3V and 4.4V, respectively. Figure 4 gives the recommended power supply connection for the circuit.

The supply currents I_A and I_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 6.3V supply voltage, I_A:

$$2.5\ \text{mA} \leqslant I_A \leqslant 4.0\ \text{mA}$$

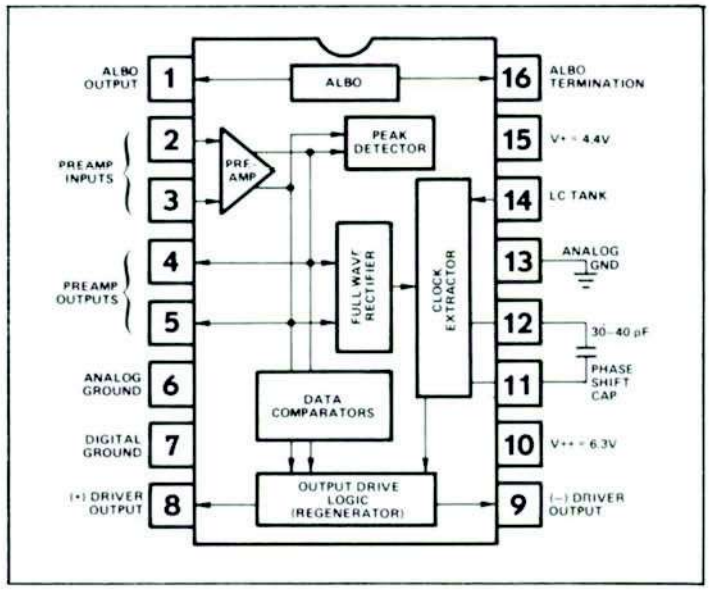

Figure 3. Package Diagram of XR-C277 Monolithic PCM Repeater

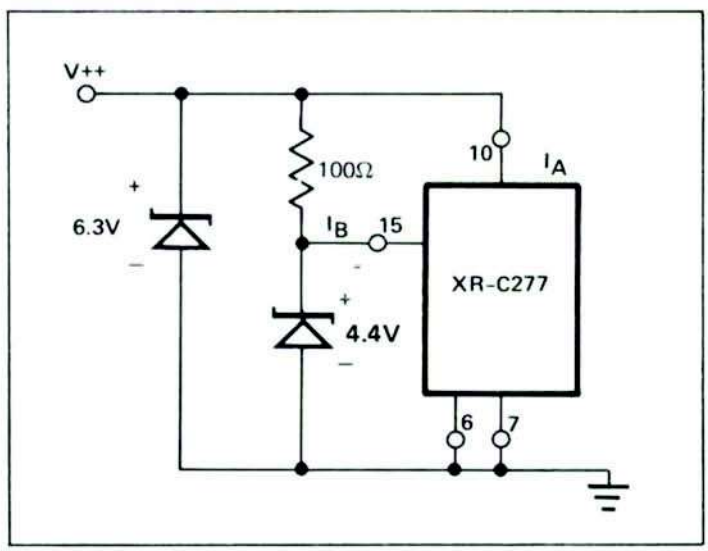

Figure 4. Recommended Supply Voltage Connection for XR-C277 (Note: See Figure 6 for Recommended Bypass Capacitors)

b. Current from 4.4V supply voltage, I_B:

$$7\ \text{mA} \leqslant I_B \leqslant 9\ \text{mA}$$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the system block diagram. Note that all the blocks shown in Figure 5 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 3).

Figure 6 shows a practical circuit connection for the XR-C277 in an actual PCM repeater application for 1.544 Mbps T-1 Repeater application. For simplification purposes, the lightning protection circuitry and the second repeater section are not shown in the figure.

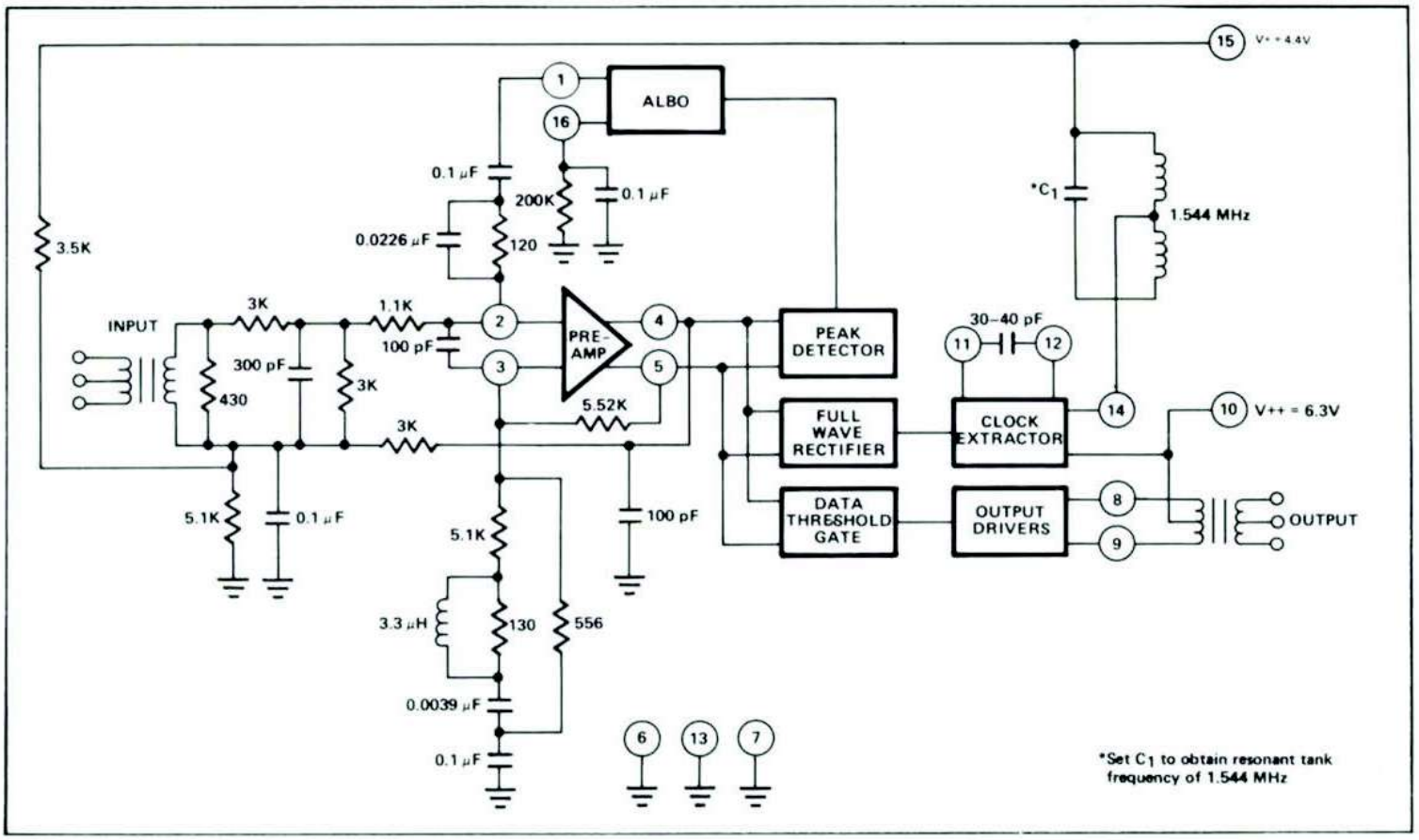

Figure 5. External Components Necessary for Circuit Operation in 1.544 MHz T-1 Repeater

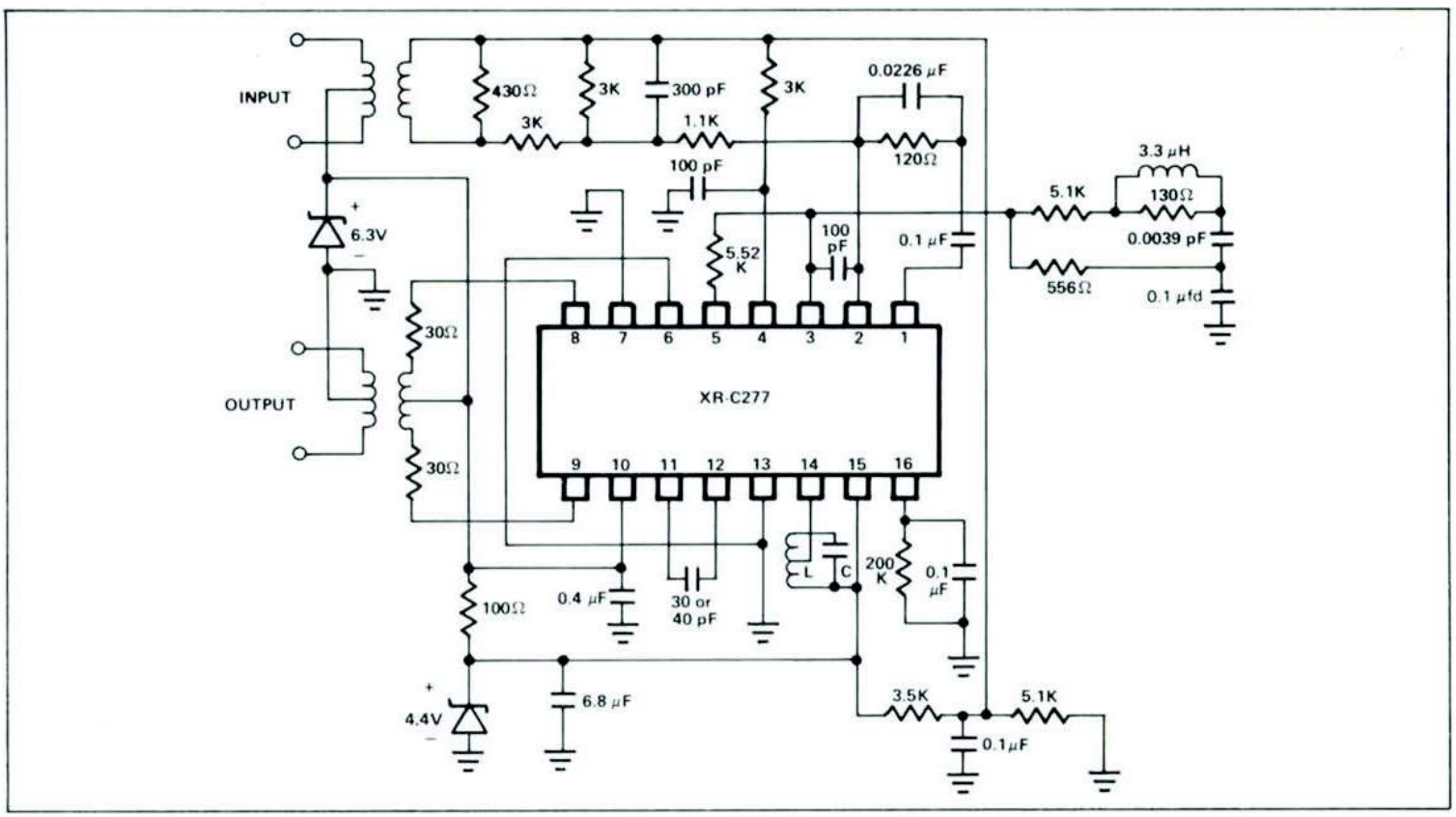

Figure 6. Typical Circuit Connection of XR-C227 in 1.544 MHz T-1 Repeater System. (Note: Set L and C to form a high Q tank resonant at 1.544 MHz. It is recommended that $Q < 100$, and $C \approx$ pF for most applications).

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Fig. 7):

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband differential voltage gain of 52 db. The differential outputs of the preamplifier (pins 4 and 5) are internally connected to the peak-detector, full-wave rectifier and the data threshold detector sections of the XR-C277.

Automatic Line Build-Out (ALBO) Section (Fig. 8):

The ALBO function is achieved by controlling the dynamic impedance of ALBO diodes (Q_{21} and Q_{22}). The current whic sets this dynamic impedance is supplied through Q_{21} and is controlled by the peak-detector output level applied to base of Q_{23}.

Data-Threshold Detector; Full-Wave Rectifier and Peak Detector Sections (Figure 9):

The level detector and peak rectifier sections of the XR-C277 are made up of two sets of gain stages which are driven differentially with the (A^+) and (A^-) outputs of the preamplifier section. The outputs of the data threshold comparators, D^+ and D^- activate the data latches shown in Figure 11.

The peak-detector output (terminal B of Figure 9) is internally connected to the Automatic Line Build-Out (ALBO) section of the circuit and controls the DC bias current through the ALBO diodes Q_{21} through Q_{22}, as shown in Figure 8.

The full-wave rectifier output is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (pin 14) of the injection locked oscillator. The detection thresholds of the comparators are set by the resistor chains (R_{45}, R_{47}, R_{51}, R_{55}) and (R_{46}, R_{48}, R_{52}, R_{56}). The resistor ratios are chosen such that the data threshold is 50% of the ALBO threshold; and the clock extractor threshold is 73% of the ALBO threshold.

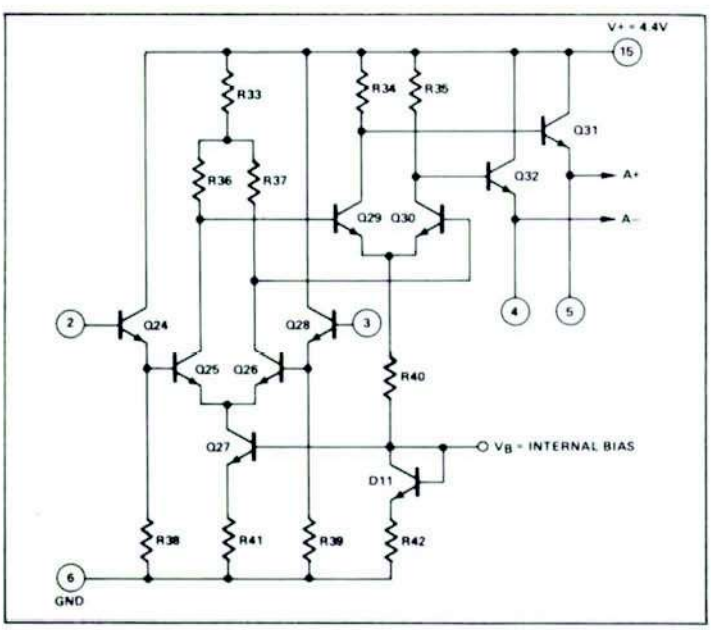

Figure 7. Circuit Diagram of Preamplifier Section

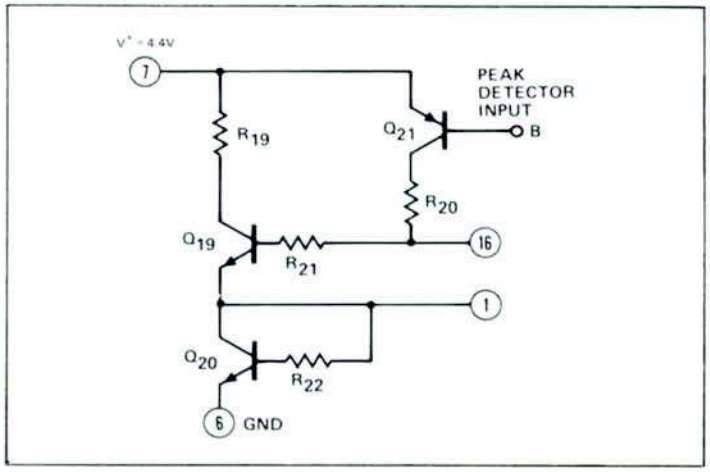

Figure 8. Automatic Line Build-Out (ALBO) Section

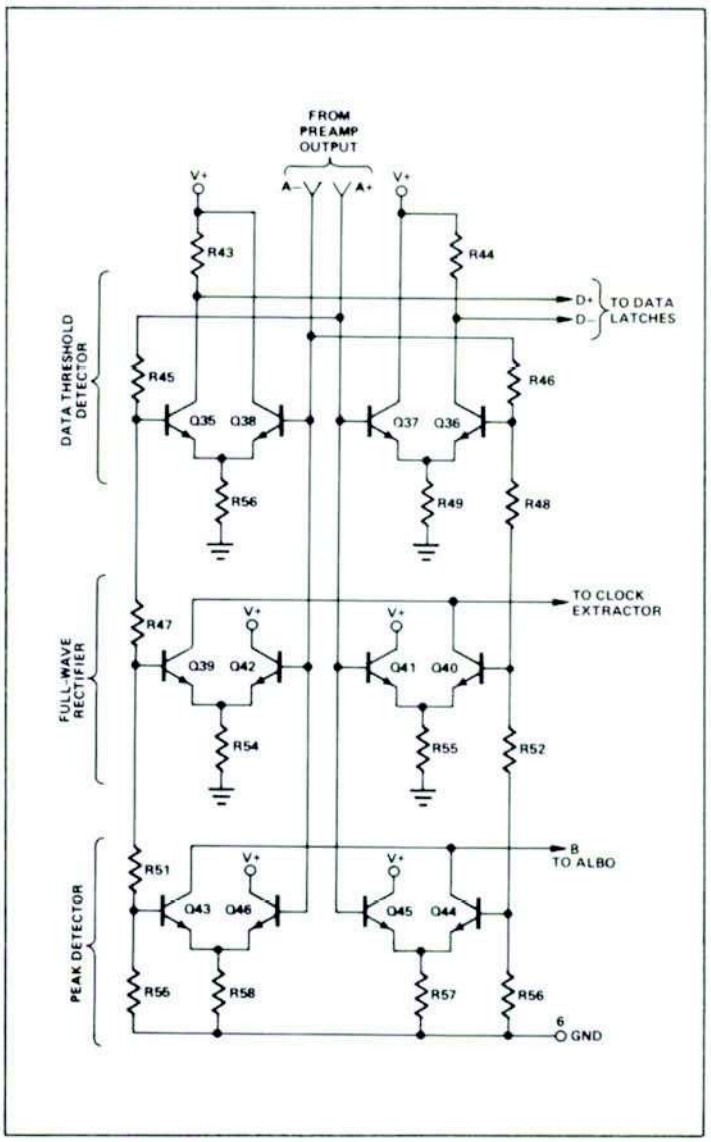

Figure 9. Data-Threshold Detector, Full-Wave Rectifier and the Peak Detector Sections of XR-C277

Clock Extractor Section (Figure 10):

The clock-extractor section of XR-C277 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{1B}, from the output of the full-wave rectifier. This signal in turn controls the current in the resonant L-C tank circuit connected to pin 14. The sinusoidal waveform across the tank is then amplified and squared through two cascaded differential gain stages made up transistors Q_3 through Q_9. The output swing of the second gain stage is "integrated" by the phase-shift capacitor, C_1, externally connected to pins 11 and 12. (See timing diagrams of Figure 13.) The nominal value of this capacitor is in the 30 to 40 pf range. The triangular waveform across pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the "strobe" signal, C_p, and the clock pulse C_ϕ, which are applied to the data latches of the logic section.

Data-Latch and Output Driver Sections (Figures 11 and 12):

The data-latch section consists of two parallel flip-flops, driven by the (D^+) and (D^-) inputs from the data-threshold detector. When the D+ input is at a "low" state, the sampling or strobe pulse, C_p, is steered through Q_{47A} and sets flip-flop 1, on the leading edge of C_p. Conversely, when D^- input is at a "low" state, the sampling pulse is steered through Q_{47B} to set flip-flop 2. Each flip-flop section is then reset at the trailing edge of the clock pulse input, C_ϕ. The flip-flop outputs, (F_1, $\bar{F}_1$) and (F_2, $\bar{F}_2$) are then used to drive the output drivers. This logic arrangement results in an output pulse width which is the same as the extracted clock pulse width (see timing diagram of Figure 13).

The outputs of the two data latches drive the two output driver stages shown in Figure 12. The high-current outputs of the driver stage (pins 8 and 9) are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage at pin 10. The output stages are designed to work into a nominal load impedance of 100 ohms, and can handle peak load currents of 30 mA.

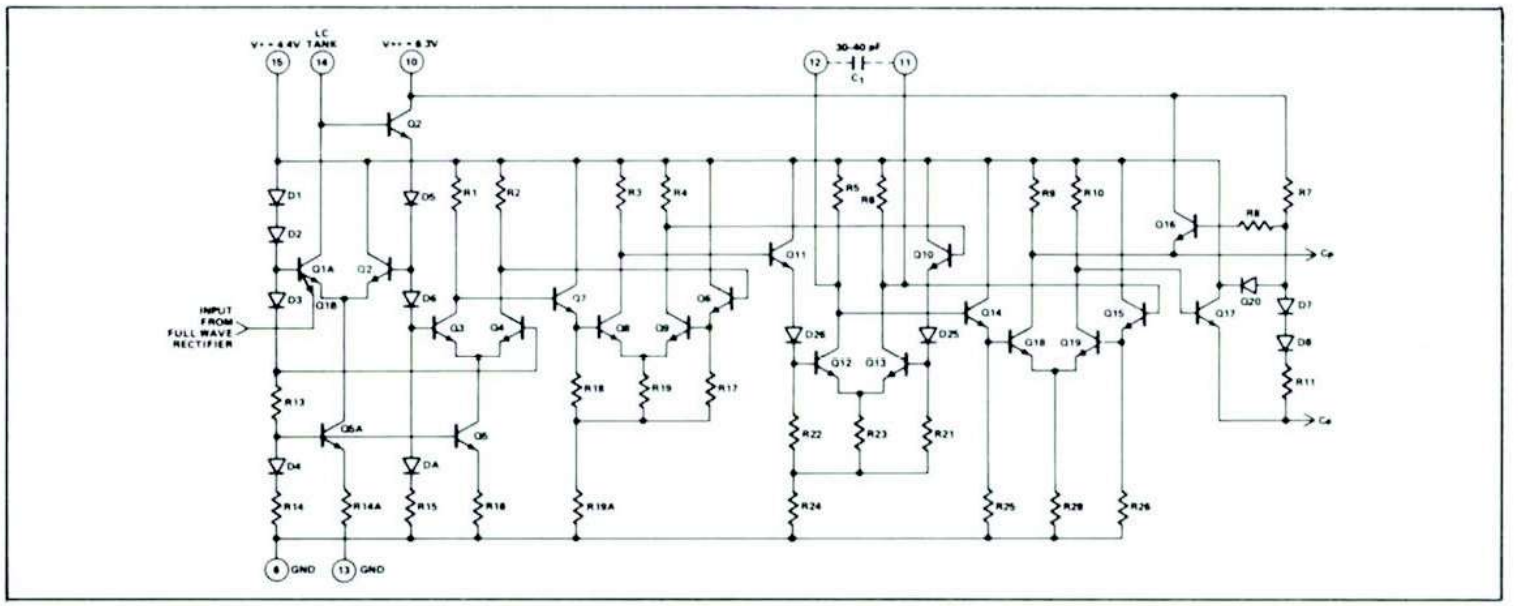

Figure 10. Circuit Diagram of Clock Extractor Section

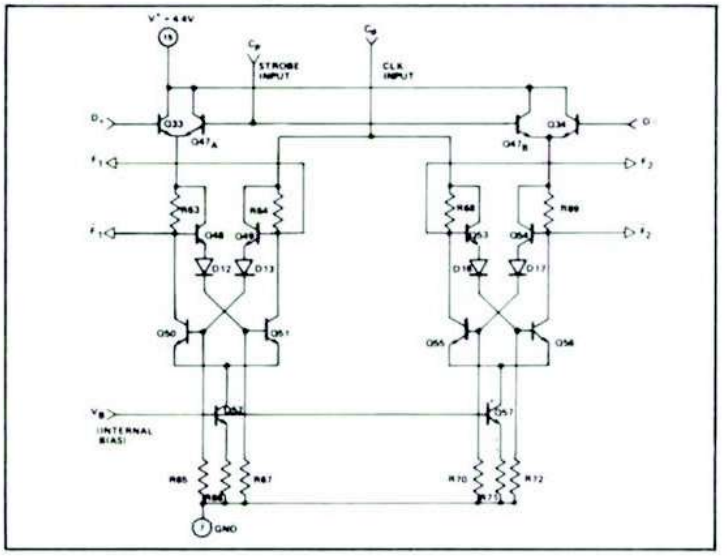

Figure 11. Data-Latch Section of XR-C277

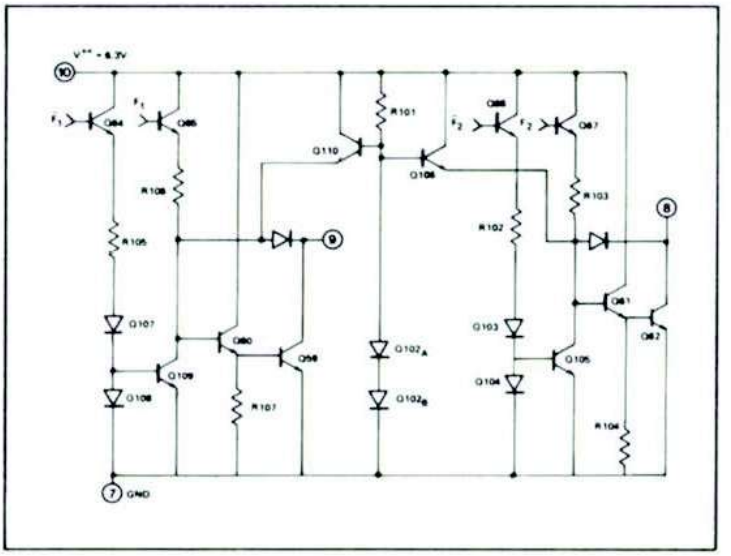

Figure 12. Output-Driver Section

Figure 13 shows the typical timing sequence of the circuit waveforms. For illustration purposes, a "one-zero-one" input data pattern is assumed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Storage Temperature Range	-65°C to +150°C

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-C277	CERDIP	-40°C to +85°C

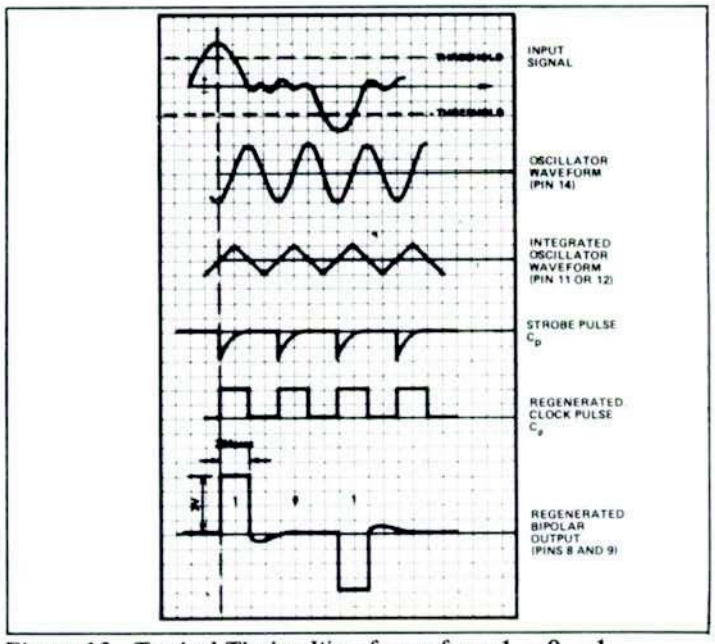

Figure 13. Typical Timing Waveforms for a 1 – 0 – 1 Input Data Pattern

ELECTRICAL CHARACTERISTICS

(+25°C, V++ = 6.3V ±5%, V+ = 4.4V ±5%, unless specified otherwise.)

PARAMETER	LIMITS				CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Supply Current					See Figure 4
I_A		3.5		mA	Measured at Pin 10
I_B		7.5		mA	Measured at Pin 15
Total Current	8	11	13	mA	$(I_C + I_B)$
Preamplifier					See Figure 7
Input Offset Voltage		1.5	15	mV	Measured at Pins 2 and 3
Input Bias Current		0.3	4	μA	Measured at Pins 2 and 3
Voltage Gain	44	48	51	dB	Single-ended gain
Preamp Output Swing					Measured at Pins 4 and 5
High Swing	3.45	3.6	3.75	V	Maximum voltage swing
Low Swing	1.25	1.4	1.55	V	Minimum voltage swing
Output DC Level	2.47	2.55	2.72	V	
ALBO Section					See Figure 8
ALBO "Off" Voltage		10	75	mV	Measured from Pin 1 and Pin 16 to ground
ALBO "On" Voltage	0.6	0.87	1.1	V	Measured at Pin 1
ALBO "On" Voltage	1.2	1.5	2.1	V	Measured at Pin 16
ALBO Threshold	1.35	1.50	1.65	V	Measured differentially across Pins 4 and 5
Differential Threshold	-75		+75	mV	Threshold difference for polarity reversal at Pins 4 and 5
ALBO "On" Impedance		5	10	Ω	Measured at Pin 1
ALBO "Off" Impedance	20	50		kΩ	Measured at Pin 1
Comparator Thresholds					See Figure 9
Clock Threshold	68	73	78	%	% of ALBO threshold
Data Threshold	47	50	53	%	% of ALBO threshold
Clock Extractor					See Figure 10
Oscillator Current	10	14	20	μA	
Tank Drive Impedance		50		kΩ	
Recommended OSC. Q	100				
$I_{injection}/I_{OSC.}$	6.0	7	7.5		Ratio of current in Q_{1B} to current in Q_{1A}
Output Driver					See Figure 12
Low Output Voltage	0.65	0.75	0.95	V	Measured at Pins 8 and 9, I_L = 15 mA
Output "Off" Current		5	100	μA	V_{out} = 20V
Output Pulse					See Figure 13
Maximum Pulse Width Error			±30	n sec	
Rise Time			80	n sec	
Full Time			80	n sec	