Institut für Nachrichtentechnik
TB

Berlin, den 20.05.1980

Bericht INT-TB 4 - 10/80

Titel: SIMPER-Katalog MOS-ED-Schaltungen

Bearbeiter: G. Heinz

Umfang: 19 Seiten

Schaltungskatalog: n-Kanal MOS ED-Schaltungen

Teil 2: SIMPER-Katalog MOS ED-Schaltungen

Dieser Katalogteil beinhaltet Schaltungen, die für die Logiksimulation mit SIMPER 5.2 (Standort: INT - SO 3) aufbereitet wurden. Die Schaltungen liegen bei SO 3 als Unternetzwerke vor.
Die Flipflop-Bezeichnungen wurden wie im ersten Katalog (Bericht INT-TB 12 - 38/78) nach der Syetematik von Stürz/Cimander[1] vereinbart.

Zu jeder Schaltung wurden

1. die MOS-ED-Schaltung
2. das Schaltsymbol
3. die im SIMPER 5.2 vorliegende Ersatzschaltung
4. die Automatentabelle bzw. die Karnaughtafel der Schaltung

angegeben. Die Anordnung erfolgte einheitlich:

1.	2.
3.	4.

Die Benennung jeder Schaltung ist 4-stellig. Die ersten drei Stellen kennzeichnen das Logikmodell, die letzte Stelle kennzeichnet die Anstieg/Abfall-Verzögerungszeit der Logikgrundgatter, eine „1" bedeutet "Einheitsverzögerung".

Spezifikationen der Verzögerungszeiten der Logikschaltungen befinden sich im Anhang. In jedes SIMPER 5.2-Modell wurden die Leitungs- und die Funktionselementnummern eingetragen, die Stiftnummerierung der Funktionselemente erfolgte generell von oben nach unten bzw. von links nach rechts und wurde nur bei Abweichung von dieser Regel vermerkt.

1) H. Stürz/W. Cimander: "Logischer Entwurf digitaler Schaltungen" VEB Verlag Technik Berlin 1976, S. 126

Bauelementebenennung:

Typ: X X X X

1. 2. 3. 4. Stelle

WIRED-Elemente

1. Stelle: Eingangsverknüpfung

AND : A NAND : N
OR : O
NEGATOR: I

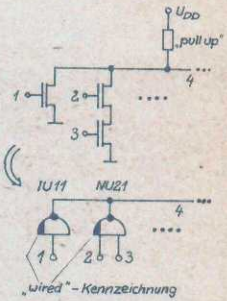
2. Stelle: Ausgangsverknüpfung

pull up : U (AND-Verknüpfung)
pull down : D (OR-Verknüpfung)

3. Stelle: Anzahl der Eingänge

4. Stelle: Verzögerungszeit

z.B.:



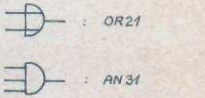
OR, AND-Elemente

1. Stelle und 2. Stelle: AND : AN
OR : OR

3. Stelle: Anzahl der Eingänge

4. Stelle: Verzögerungszeit

z.B.:

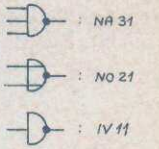


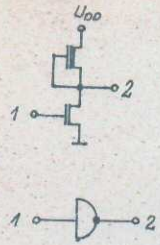
NAND, NOR, NEG-Elemente:

1. Stelle und 2. Stelle: NAND : NA
NOR : NO
NEGATOR : IV

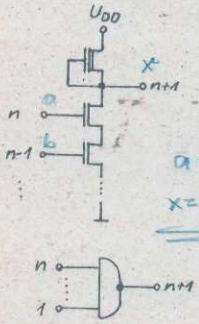
3. Stelle: Anzahl der Eingänge

4. Stelle: Verzögerungszeit

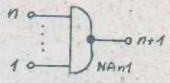




Negator **IV 11**



NAND **NA n 1** $n \leq 4$



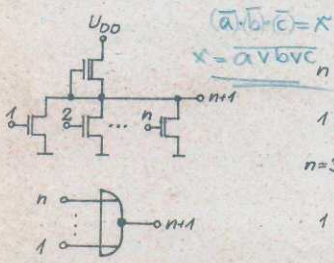
$a \cdot b = \bar{x}$

$x = \overline{a \cdot b}$

n: Anz. der Eingänge

n=3

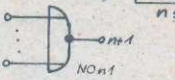
	23			
	00	01	11	10
0	1	1	1	1
1	1	1	0	1



$(\bar{a} \vee \bar{b} \vee \bar{c}) = \bar{x}$

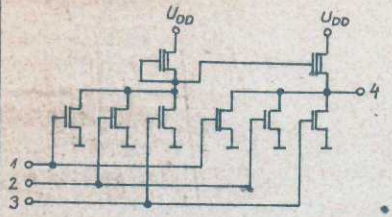
$x = \overline{a \vee b \vee c}$

NOR **NO n 1** $n \leq 6$



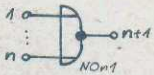
n=3

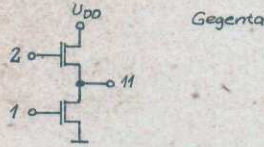
	23			
	00	01	11	10
0	1	0	0	0
1	0	0	0	0



zu **NO n1**

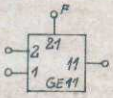
$n: 2,3$

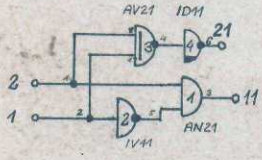


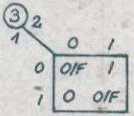


Gegentakttreiber-Enh.

GE 11



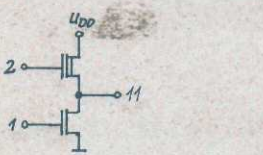




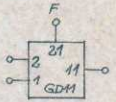
$3 = \bar{1} \cdot 2$

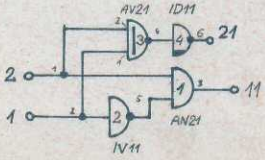
$21 = \bar{1} \cdot \bar{2} \vee 1 \cdot 2$

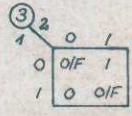
$F: 21 = „1"$



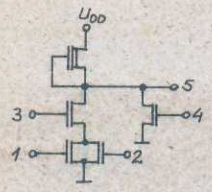
GD 11

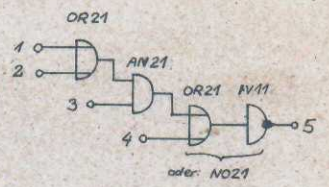




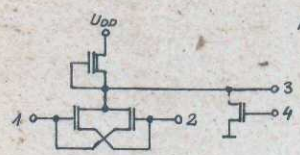


vermaschte Strukturen, nicht als Modell erfaßt: z.B.:

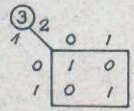


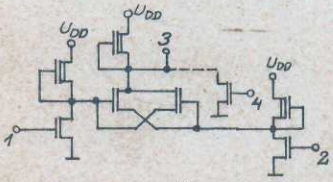


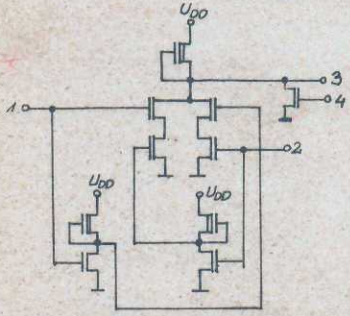
Aequivalenz **AE21**



Symbol + UNW:

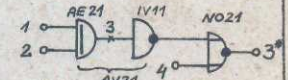


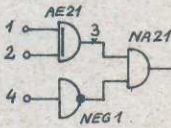




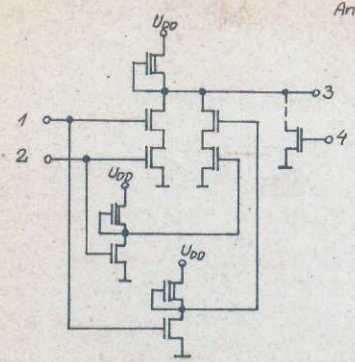
mit Erweiterung durch „4":
(nicht als Modell erfaßt)

$$3^* = \overline{3 \vee 4} = 3 \cdot \bar{4} = 1 \sim 2 \cdot \bar{4}$$

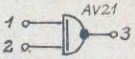




Antivalenz — AV 21

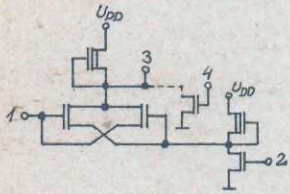


Symbol:



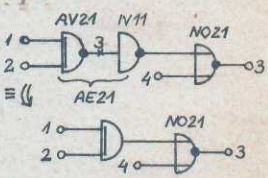
KT:

③ 2	0	1
1		
0	0	1
1	1	0

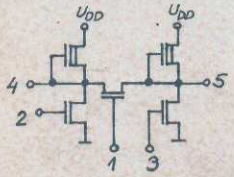


$3 = \bar{4}\,(1\bar{2} \vee \bar{1}2) = \overline{4 \vee (12 \vee \bar{1}\bar{2})}$

mit Erweiterung „4":
(nicht als UNW erfaßt)

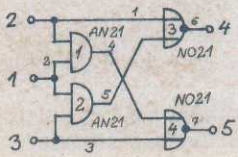


Transfergate, statisch — TG 31



Symbol:

UNW:

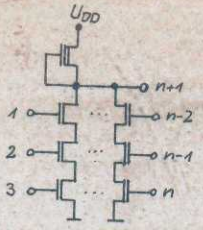


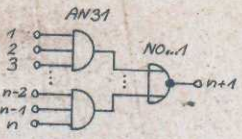
(45) 23	00	01	11	10
1				
0	11	10	00	01
1	11	00	00	00

$4 = \bar{1}\cdot\bar{2} \vee \bar{2}\cdot\bar{3}$

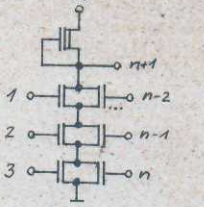
$5 = \bar{1}\cdot 3 \vee \bar{2}\cdot\bar{3}$

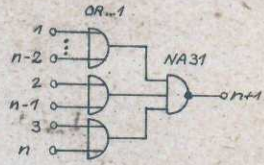
erweitertes NOR:



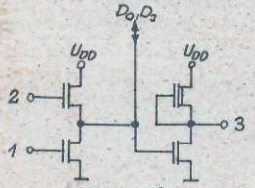


erweitertes NAND:

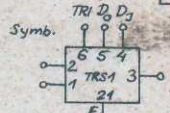




TRS 1



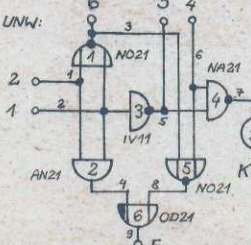
Tristate



Realschaltung:

TRI 6	D0 5	D3 4	2	1	3	
0	0	–	0	1		Eingabe
0	0	–	1	0		Eingabe
1	0	0	–	1		Ausgabe
0	1	1	–	0		Ausgabe
1	1	–	–	–		verboten (F)

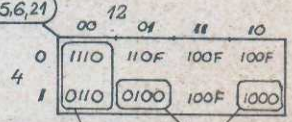
UNW:



$F = 21 = 1 \cdot 2 \vee \overline{4}\,(1 \vee 2)$

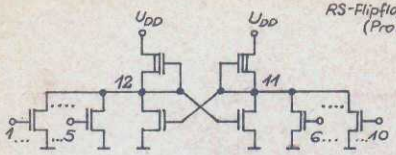
3,5,6,21

KT:

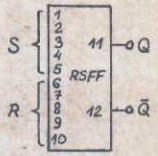


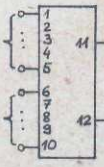
RS-Flipflop; Grundzelle (Prozedur)

RS 11

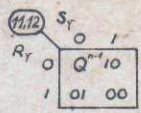


Symbol

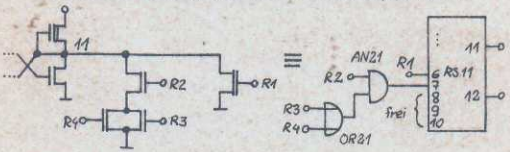




AT:

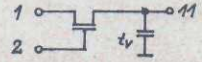


mögliche Erweiterungen, die nicht im Modell erfaßt sind:



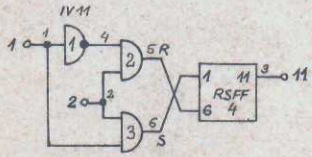
DV-Flipflop; statisch bis t_V

DV11

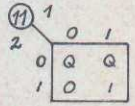


Bem: Q nach t_V undefiniert.

Symbol:

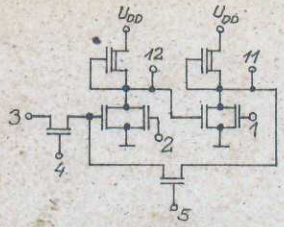


AT:

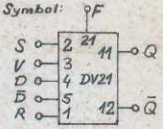


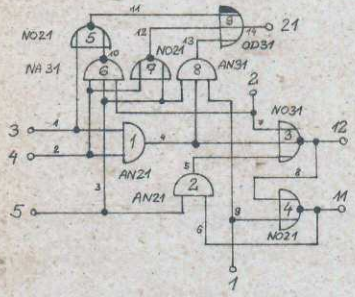
Bem: Modell statisch, ohne t_V!

DV- Flipflop **DV21**



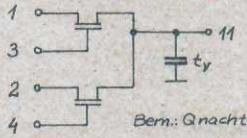
Symbol:





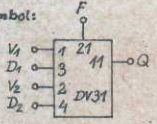
11,12,21	1,2			
4,5	00	01	11	10
00	01F	100	000	010
01	Q$\bar{Q}$0	100	000	010
11	01F	00F	00F	010
10	010	100	000	010
10	100	100	00F	000
11	10F	10F	00F	00F
01	Q$\bar{Q}$0	100	000	010
00	01F	100	000	010

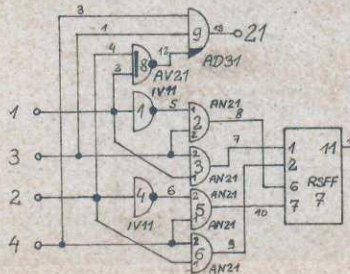
DV- Flipflop **DV 31**



Bem.: Q nach t_y undefiniert

Symbol:

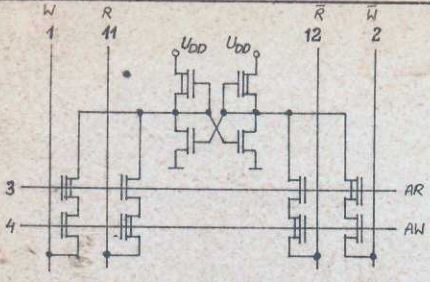


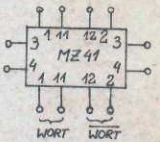


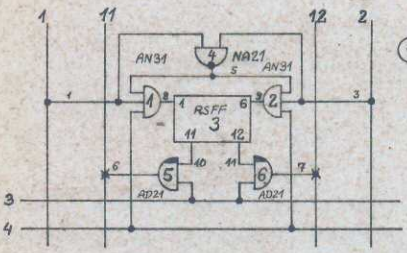
11	1;2			
AT: 3,4	00	01	11	10
00	Q	Q	Q	Q
01	0	1	1	0
11	0	1F	1	1F
10	0	0	1	1

Bem.: Modell statisch, ohne t_y.

MZ41







11,12 \ 3,4 / 1,2	00	01	11	10	
00	00	00	F	F	
01	00	00	01	Q	← W
11	00	00	Q	Q	← R
10	00	00	10	Q	← W

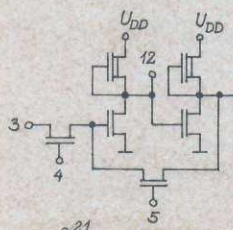
Bem:

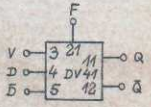
*: „pull down"-Leitung (OR-Typ)

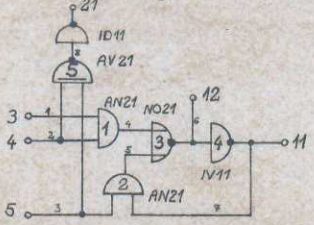
F: Nichtübereinstimmung zu Schaltung und Logik.

DV41

DV-Flipflop



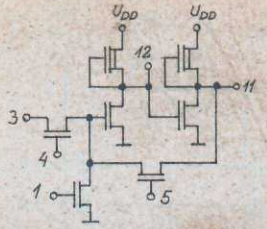


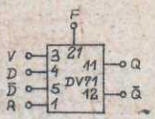


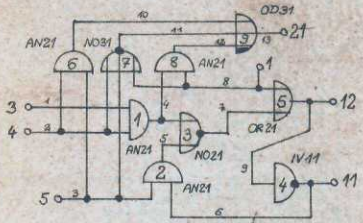
11,12,21 \ 3 / 4,5	0	1
00	F	F
01	Q	Q
11	F	F
10	01	10

DV 71

DV- Flipflop



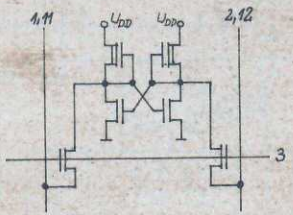


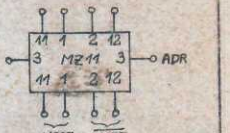


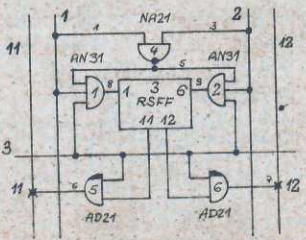
11,12,21 / 4,5	3,1 00	01	11	10
00	F	01	01	F
01	Q	01	01	Q
11	F	F	F	F
10	01	01	F	10

MZ11

Speicherzelle







11,12 / 1,2	3 0	1
00	Q	F
01	Q	01
11	Q	Q
10	Q	10

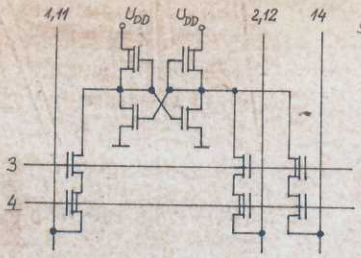
lesen
schreiben

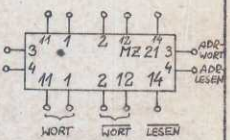
F: Fehler werden aus Redundanzgründen durch Schreibverstärker (-5V...) angezeigt.

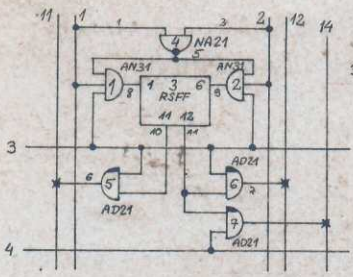
* „pull down" (OR-Typ)

Speicher-zelle

MZ 21







11,12,14 / 1,2 / 3,4

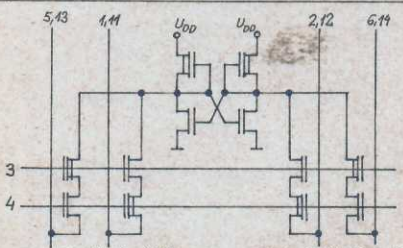
3,4 \ 1,2	00	01	11	10
00	000	000	000	000
01	00$\bar{Q}$	00$\bar{Q}$	00$\bar{Q}$	00$\bar{Q}$
11	Q$\bar{Q}\bar{Q}$	011	Q$\bar{Q}\bar{Q}$	100
10	Q$\bar{Q}$0	010	Q$\bar{Q}$0	100

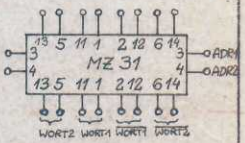
lesen — schreiben

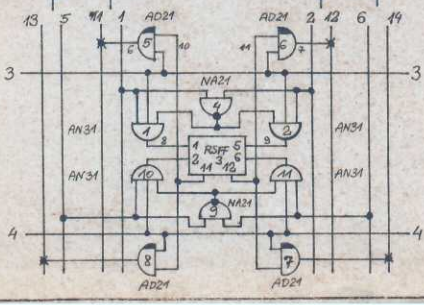
Bem:
- Fehlerausgabe vom SV
- ✶ : „pull down" (OR-Typ)

Speicher-zelle

MZ 31







11,13 / 1,5 / 3,4

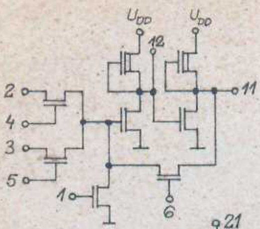
3,4 \ 1,5	00	01	11	10
00	00	00	00	00
01	0Q	01	01	0Q
11	QQ	11	11	11
10	Q0	Q0	10	10

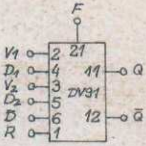
lesen: 1·2·5·6 = „1"

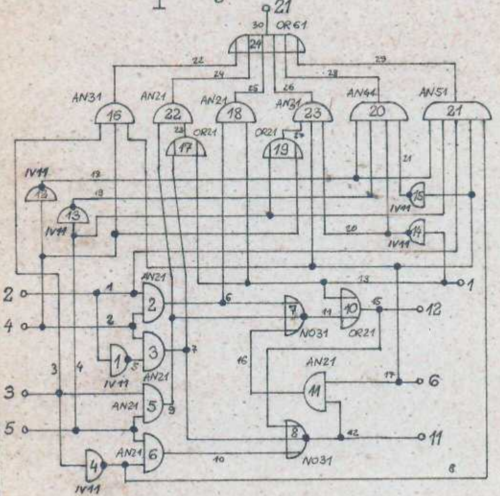
Bem:
- Fehlerausgabe vom SV
- ✶ : „pull down" (OR-Typ)

DV-Flipflop

DV91.



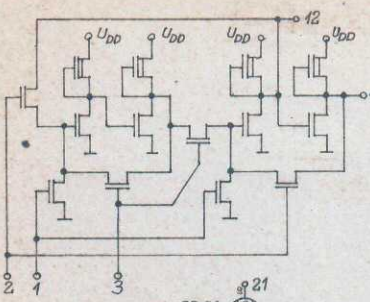


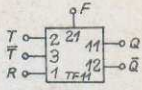


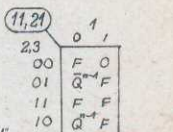
11,12,21 (4,5 \ 2,3)	6 = 0: 00	01	11	10	6 = 1: 10	11	01	00
1 = 0: 00	F	F	F	F	$Q\bar{Q}$	$Q\bar{Q}$	$Q\bar{Q}$	$Q\bar{Q}$
01	01	10	10	01	F	F	F	F
11	01	F	10	F	F	F	F	F
10	01	01	10	10	F	F	F	F
1 = 1: 10	01	01	F	F	F	F	F	01
11	01	F	F	F	F	F	F	01
01	01	F	F	01	F	F	F	01
00	01	01	01	01	01	01	01	01

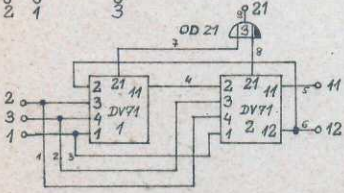
Teiler-FF

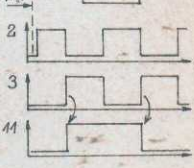
TF11





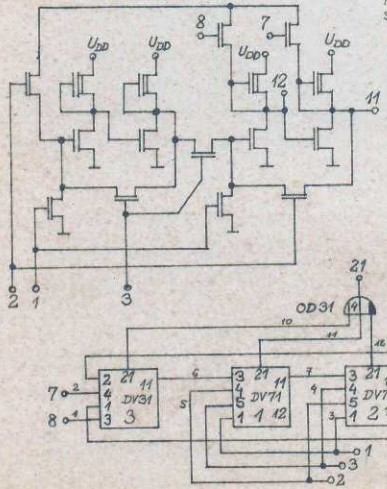


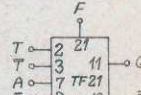


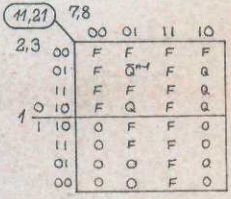


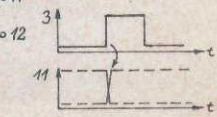
Teiler-FF, steuerbar

TF21



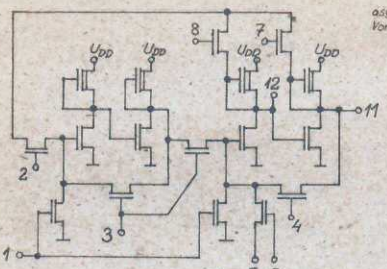


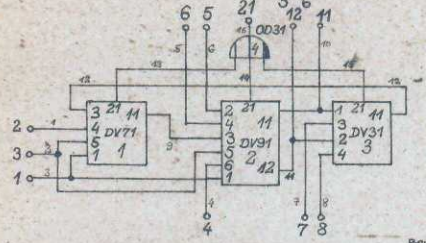




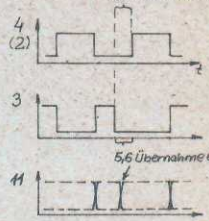
asynchrone Voreinstellung

TF 31





5,6-Übernahme mögl.



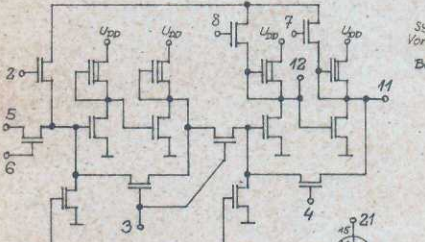
Bem.: 5 einschreiben: 3V4V1 = „0"

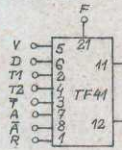
- verboten: 1·5·6 = „1" ; 7·8 = „1" ; 1·2·7·11 = „1" ; 1·2·8·12 = „1" ; 4·6 (5 = „1") = „1"
- allg. Bed.: 3·4V4·6V3·6 = „0"
- Vorsicht bei 3·5·6 = „1" !

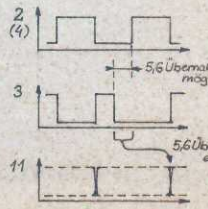
TF 41

Synchrone Voreinstellung

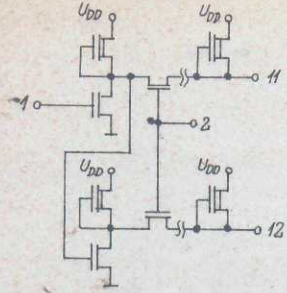
Bem.: • 5 einschreiben: 1V2V3 = „0"

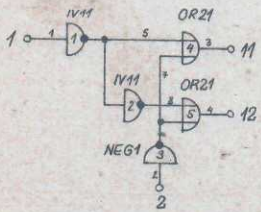


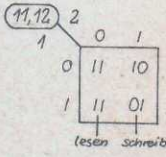




Schreibverstärker **SV 11**



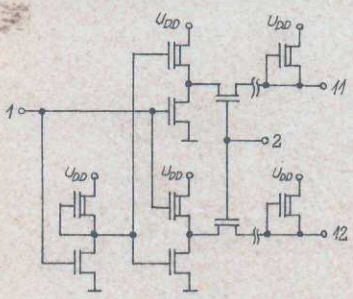


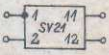


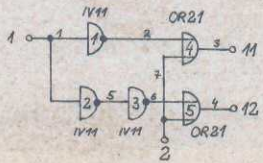
$11 = \bar{1} \vee \bar{2}$

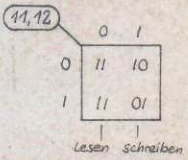
$12 = 1 \vee \bar{2}$

SV 21



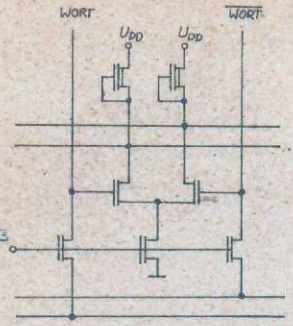




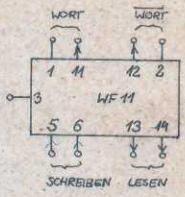


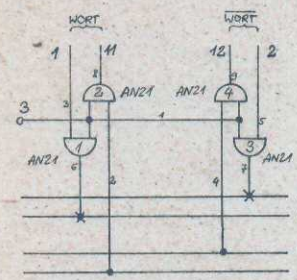
$11 = \bar{1} \vee \bar{2}$

$12 = 1 \vee \bar{2}$



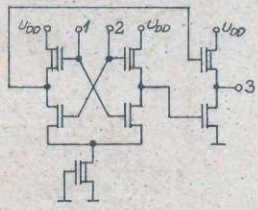
Wortfreigabeschaltung WF 11



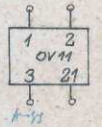


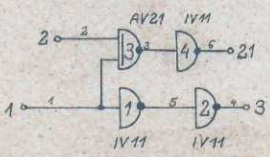
11 = 3·5
12 = 3·6
13 = 3·1
14 = 3·2

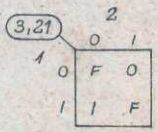
Bem:
✱ : OR-verknüpfen (13, 14)



Leseverstärker OV 11

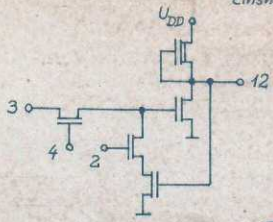


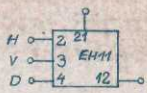


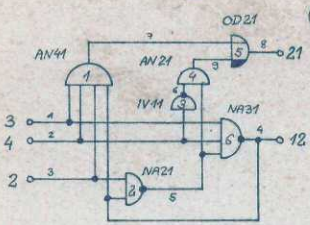


Einshalteflipflop

EH 11







12,21 $\quad 2, 12^{(t-1)}$

3,4	00	01	11	10
00	1F	1F	1	1F
01	1	1	1	1
11	0	0	0F	0
10	1F	1F	1	1F

Bem.: 3·4·2·12 = 0F wird als 1F ausgegeben !!