Flipflop - Typen

(H. Stöhr, U. Giesecke: Logischer Entwurf digitaler Schaltungen. VT 86, 1986, S. 126)

(Antivalenz-Latch)

RS-Flipflop

R^n	S^n	y^n
0	0	y^{n-1}
0	1	1
1	0	0
1	1	–

JK-Flipflop

J^n	K^n	y^n
0	0	y^{n-1}
0	1	0
1	0	1
1	1	$\bar{y}^{n-1}$

DV-Flipflop

D^n	V^n	y^n
0	0	y^{n-1}
0	1	y^{n-1}
1	0	0
1	1	1

SL-Flipflop

S^n	L^n	y^n
0	0	y^{n-1}
0	1	0
1	0	1
1	1	1

EL-Flipflop

E^n	L^n	y^n
0	0	y^{n-1}
0	1	0
1	0	1
1	1	0

Teilerflipflop

T^n	y^n
0	y^{n-1}
1	$\bar{y}^{n-1}$

Aequiv. Latch

A	B	Q^n
0	0	0
0	1	Q^{n-1}
1	0	Q^{n-1}
1	1	1

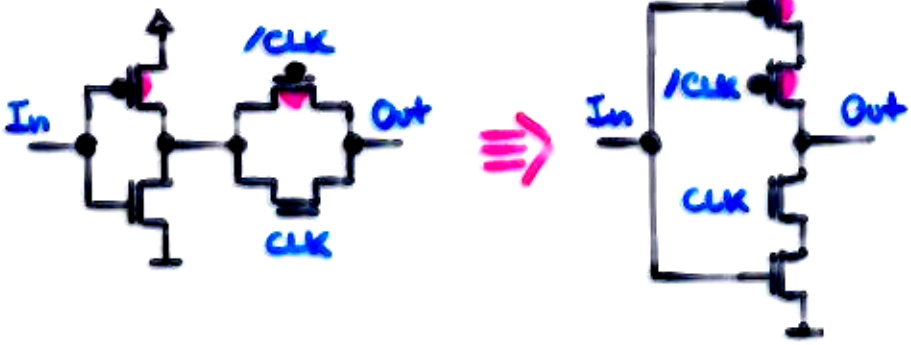
D-Latch; DFF

D^n	y^n
0	0
1	1

Der Hochstrich kennzeichnet die [illegible]

C^2MOS – Latches & Flipflops

C^2MOS-Latch:



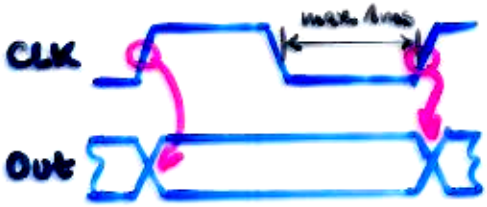
Vorzüge:

- layoutgünstig (n = p)
- aktiv pegelregenerierend

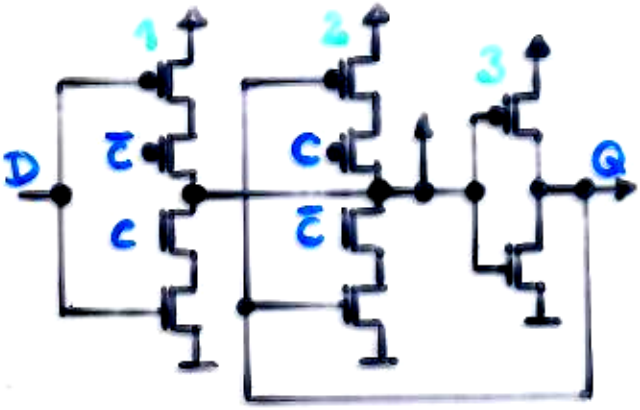
Gestaltung:
Inverter empfindlicher bei Charge sharing-Gefahr.

C^2MOS-Latch als dyn. D-Latch:

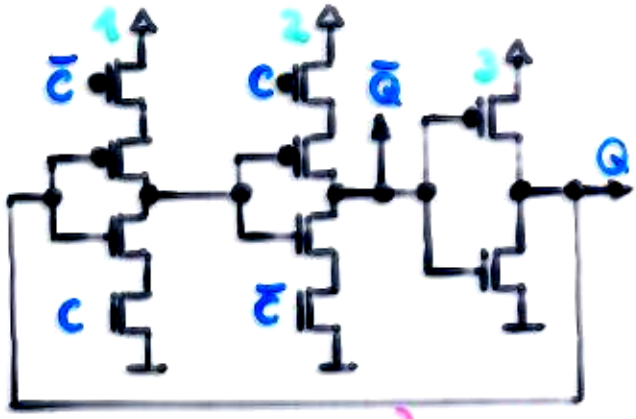
$(In = \bar{D})$



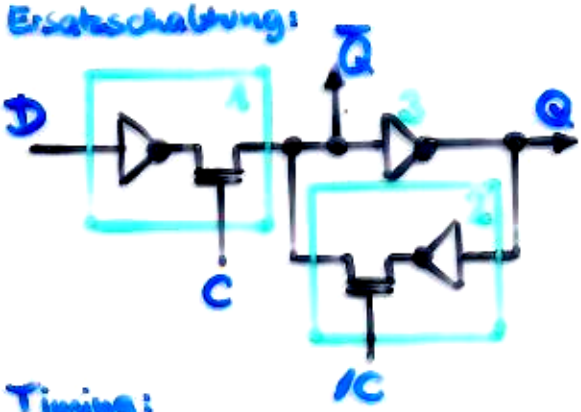
Statisches D-Latch (LM1500 "LATCH")

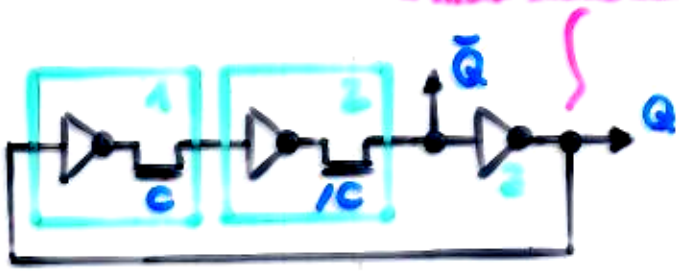


dyn. Teiler-Flipflop (LM1500 "DYNTFF")

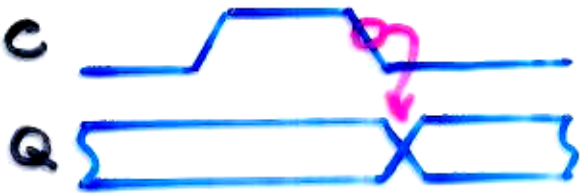


Ersatzschaltung:



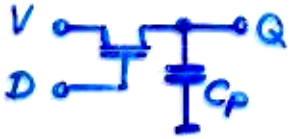


Timing:



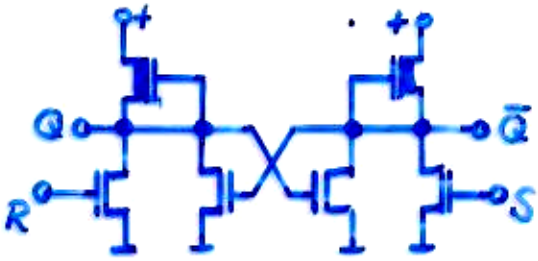
$f_{min} \geq 1\,kHz$

dynamisches DV-Latch

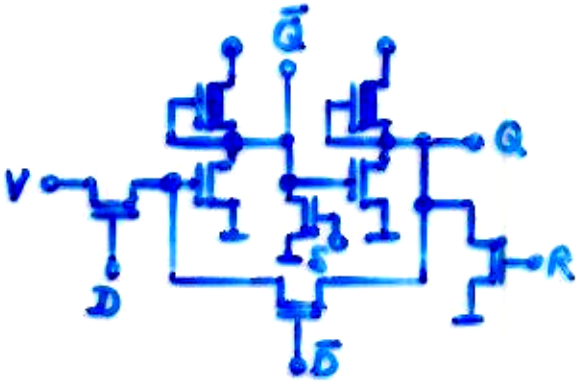


D^n	V^n	Q^n	
0	0	Q^{n-1}	} max. 2ms „H"
0	1	Q^{n-1}	
1	0	0	
1	1	1	

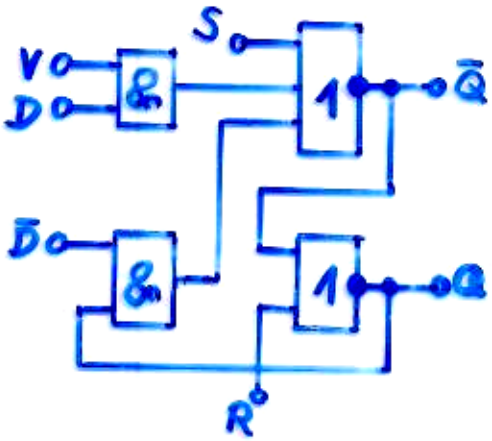
RS-Latch



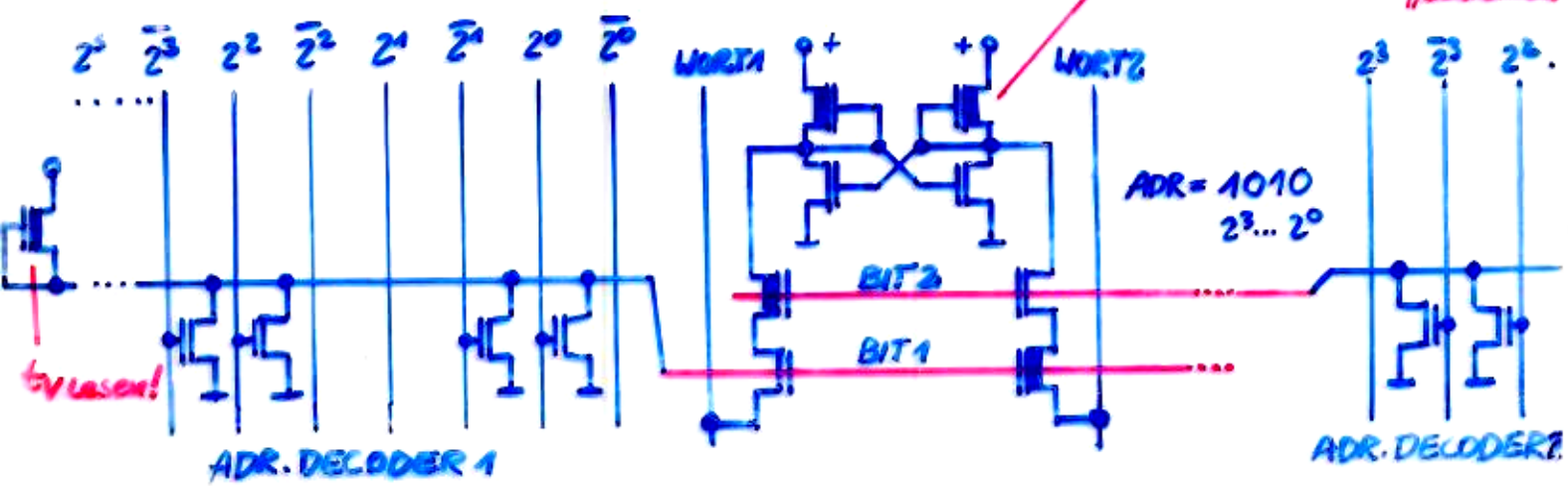
statisches DV-Latch



DV-Ersatzschaltung (SIMPER)



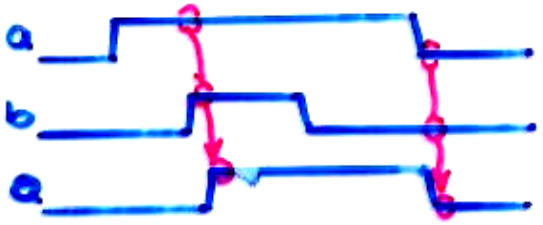
Speicherzelle mit Adreßdecoder (2-fach)

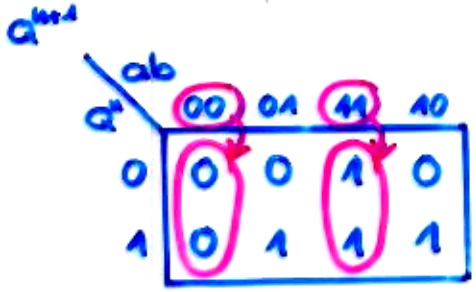


$J_{A0} = \left(\frac{b}{c}\right)_{Last}$: $A, t_V \leftrightarrow P_V$ „schreiben"

Äquivalenzlatch (Muller-C-Element /MC80/ S. 254)

Zeit:

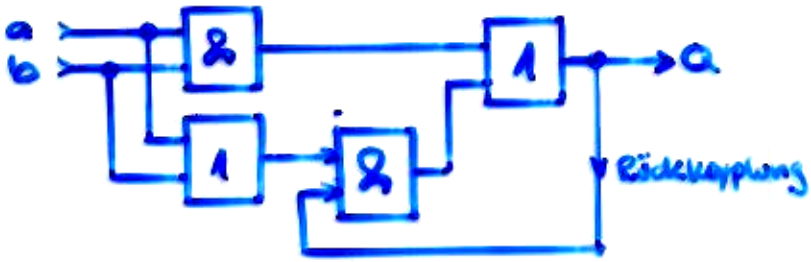




a	b	Q^{n+1}
0	0	0
0	1	Q^n
1	0	Q^n
1	1	1

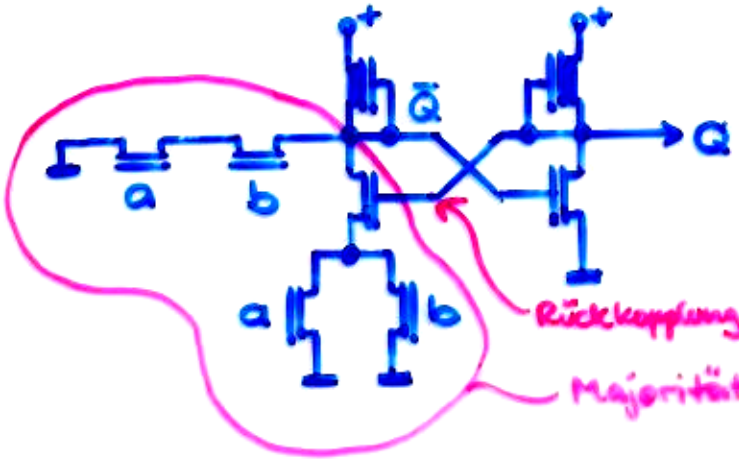
Funktion:

Ersatzschaltung:



Realisierung:

praktischer Aufbau (NSGT):

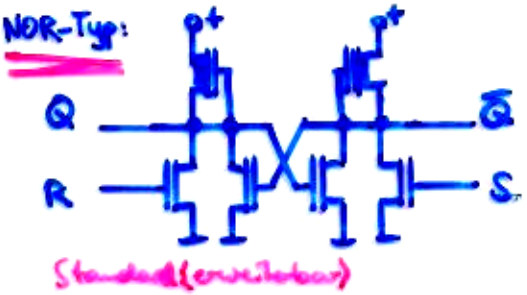


Gesichte

Eigenschaft: assoziativ:
(Vorgänger)

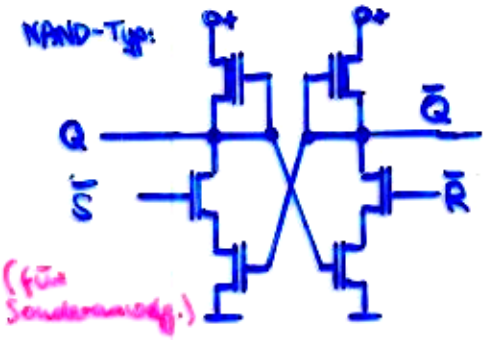
RS-Latches:

NOR-Typ:



Standard (erweiterbar)

NAND-Typ:



(für Sonderanwendg.)

Unterschied:

NOR-RS:

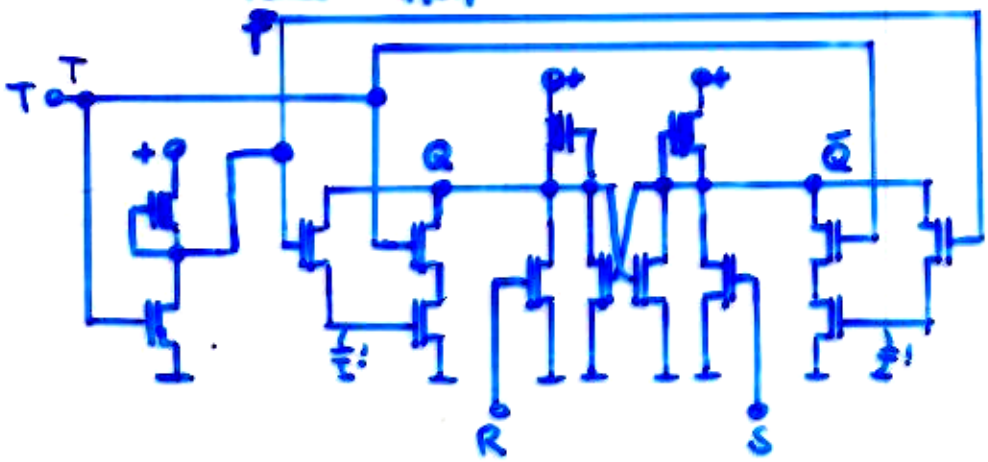
Q,$\bar{Q}$	S=0	S=1
R=0	Q,$\bar{Q}$	10
R=1	01	00

NAND-RS:

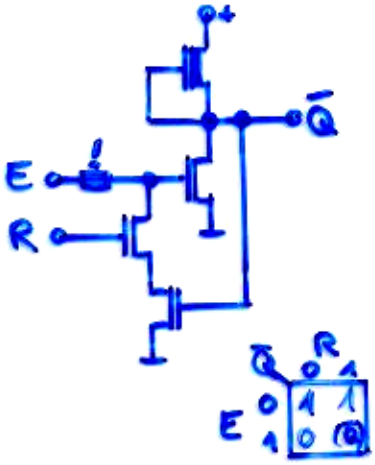
Q,$\bar{Q}$	$\bar{R}$=0	$\bar{R}$=1
$\bar{S}$=0	11	10
$\bar{S}$=1	01	Q,$\bar{Q}$

!

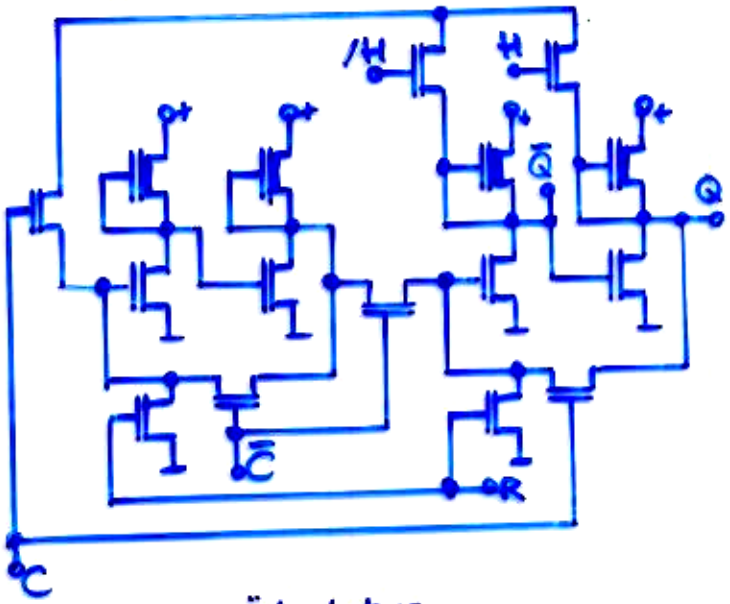
Teiler-Flipflop:



Einshalter:

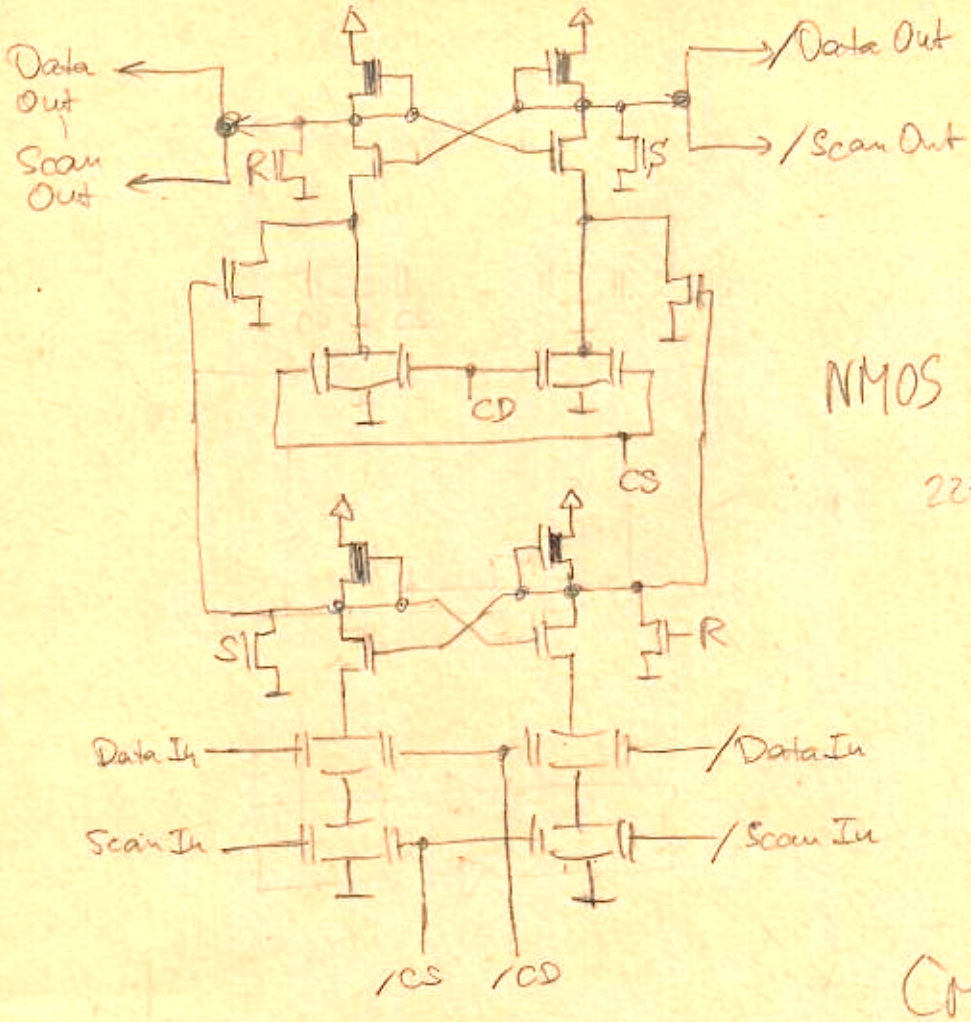


Teilendes JV-Master-Slave-FF:



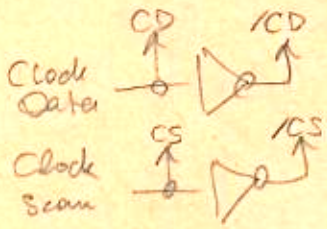
- rücksetzbar
- teilen/nicht teilen-Mode

Doppeltakt - SRFF in NMOS



NMOS ✓

22Trs



CMOS