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CELL BASED DELAY ANALYSIS WITH FINITE TRANSITION SLOPES

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The article offers a simple method and some results to measure dynamic characteristics at digital MOS-gates with respect to finite transition slopes (endliche Flankensteilheiten) at the in- and outputs of gates. Measurement conditions are discussed. Gates are considered as cell based black boxes. Some fundamental physical properties are shown. Rules for measuring delay schemes are developed. An algorithmic idea for a core of a class of new, extremely fast and accurate timing verifiers is given.

KEY WORDS Integrated circuit design, timing verification, logic simulation, delay vector, delay scheme, dynamics of digital MOS gates.

1. INTRODUCTION

In [6] published circuit simulations had shown, that a delay of a CMOS gate, *driving equal loads,* but being driven under different input slopes *can differ in the range of* 1 *to* 300 from the quasi static to the step response. Additional delays are influenced on variations of power supply, temperature and geometrical ratios. This fact makes it *theoretical* nearly impossible, to use Elmores RC-delay [1] for modelling the delay of digital gates in a zero/one logic simulation environment. So in practice different, mostly difficult methods had been developed to increase the precision of dynamic modelling [9] compared with logic simulation and to reduce the necessary computation time compared to circuit simulation.

Ignoring *transition slopes at nodes* as main parameters, allround logic simulators operate with a high dynamic fault possibility risk. RC-based 'average' delay estimations will not avoid dynamic, steepness produced errors on nodes laying anywhere on a critical path in a circuit. Hence, designs actual done without circuit simulation have dynamical lacks. Present logic verification methods that are oriented at RC-based delay models are of limited worth. A more closed dynamic verification ought to make the yield and the reliability of integrated circuits some percents higher, especially in the field of the beginning high speed and large integrated video-communication industry. According to [8] the article shows how to design easy and compact cell based gate models useable for logic simulation including transition slopes. Thus the ideas presented here are of some general interest for new kinds of very precious and fast together cell based, *iterative* working timing verifiers as well as for straight forward, *event oriented* logic simulators.

2. INTERPRETING DIGITAL TRANSITIONS

It is possible, to expand any digital waveform $v(t)$ into a power series at a reference point (v_k, t_n). For a digital transition this can be done in the Taylorian power series form at the reference voltage v_k and the reference time t_n, compare Figure 1.

$$v(t) = v_k(t_n) + \frac{v_k'(t_n)}{1!}(t - t_n) + \frac{v_k''(t_n)}{2!}(t - t_n)^2 \tag{1}$$

For practical use it is important, to consider the first two terms of the right side. All voltages V are normalized on the signal swing V_{hub}, $v = V/V_{\text{hub}}$. Changing a reference voltage at any transition than has the limit

$$\lim_{t \to t_n} \frac{v(t) - v(t_n)}{t - t_n} = v'(t_n) \tag{2}$$

To simplify the writing, in accordence to [7] and [8] the derivative $v'(t_n)$ is

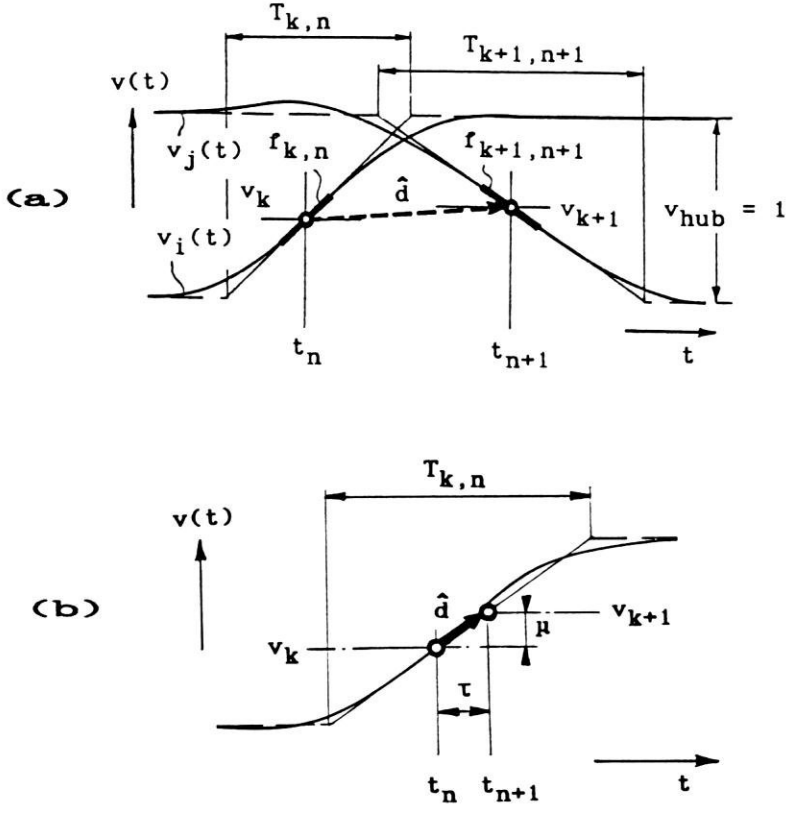


Figure 1 Input and output transitions at an inverter (a) and inside a node (b). Different reference voltages supposed the delay appears as vector $\hat{d}$.

shortened to the so called *transition slope* f (Flankensteilheit). The *transition duration* T (Flankendauer) appears as the inverse of f.

$$v'(t_n) = f = 1/T \tag{3}$$

Figure 1 shows any two transitions with different reference (measurement-, threshold-) levels (voltages). Between both transitions occurs a *delay* τ together with a *reference level shift* μ (without dimension).

$$\tau = t_{n+1} - t_n \tag{4}$$

$$\mu = v_{k+1} - v_k \tag{5}$$

Because τ and μ ever appear together, they built a *delay vector* $\hat{d}$.

$$\hat{d} = (t_{n+1} - t_n)\hat{t} + (v_{k+1} - v_k)\hat{v} = \tau\hat{t} + \mu\hat{v} \tag{6}$$

$\hat{t}$ and $\hat{v}$ are the unit vectors of the time- and voltage axis. Comparing the slopes of two transitions it is possible to define a *transition ratio* p (Flankenverhältnis) between any two transitions f_a, f_e.

$$p = f_{n+1,k+1}/f_{n,k} = f_a/f_e \tag{7}$$

Reference voltages v are connected with geometrical places at the scheme (index k). Time steps are connected with time coordinates (index n). Thus the transition slope f includes place and time coordinates together. According to Figure 1 the index 'out' means $n+1$, $k+1$ and 'in' is n, k.

If a simple node exists in a circuit, being measured to different directions in the circuit with different reference voltages, this *node gets more than one voltage and time reference.* As proportion between the inner nodal reference shift μ and the inner nodal delay time τ one can find the *transition time* T (source [6]).

$$T = (t_{n+1} - t_n)/(v_{k+1} - v_k) = \tau/\mu \tag{8}$$

Thus, every node in a delay scheme can get a delay time: Graphs of a logic scheme and a corresponding delay scheme of one circuit are unique reflective (eindeutig abbildbar), but can not be equal.

3. REFERENCE LEVELS AT GATES

A static transfer diagram (Figure 2) of any And- Or- Invert (AOI-) gate shows, that different inputs can have different static transfer curves $V_a(V_e)$. For very slow transition slopes (t.m. for $f_e \to 0$) the measurement of delays at the gate input is only possible holding the static output current I_0 at zero. Therefore it's *impossible, to measure a gate with more than one input with equal reference voltages at all inputs and outputs* (for instance at VDD/2). Figure 2 illustrates this case. To introduce delay vectors it is necessary to model the gate timing in a correct way.

Figure 2 shows also another problem using real gates. Suppose, we turn the horizontal broken line (V_{0a}) creating the reference voltages of the inputs (V_{0e}) to a diagonal position, as proposed by Mead [2]. Then the output gets three different reference voltages produced from three different inputs. Any timing

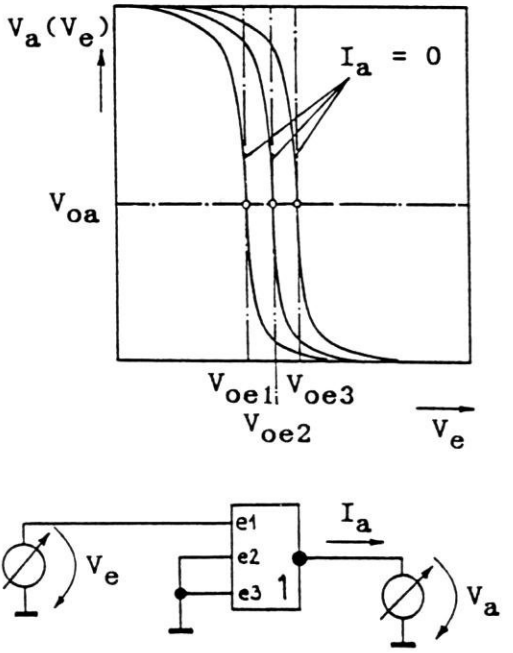


Figure 2 NOR3 static gate diagram. The choice of reference voltages is restricted to $I_a = 0$ curves.

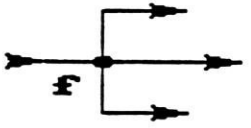
calculation going on to some following nodes would have to check up this different cases. To choose the reference voltage of a gate easier, it is necessary to start from the output node and to *create one reference voltage at every input.* Then logical or functional dependencies between references and events are avoidable. In difference to [2] it seems impossible, to introduce other than horizontal lines creating reference voltages for MOS gates.

4. RULES FOR DELAY SCHEMES

For the practical work with Taylor transitions in [7] one can find first time some plausible rules and definitions.

Node

A node in a delay scheme is not allowed to have a delay. The reference level shift has to be zero. The transition slopes f at inputs and outputs are equal, thus the transition ratio p is one.

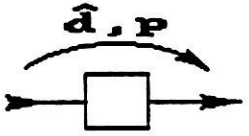


$$\hat{d} = 0 \tag{9}$$

$$p = 1 \tag{10}$$

Branch

Between input and output of a branch exists a delay vector, consisting of a level shift μ and a delay τ. A branch can own any transition ratio p between output and input transition.

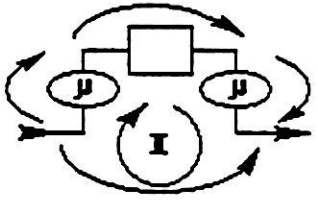


$$\hat{d} = \tau\hat{t} + \mu\hat{v} \tag{11}$$

$$p = f_a/f_e \tag{12}$$

Mesh

The sum of all branch delays $\hat{d}_i$ along a closed mesh I has to be zero. The product of the transition ratios p of all included branches is one, suggested all transitions have the same source.

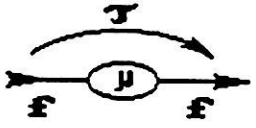


$$\hat{d} = \sum_{i=1}^{m} \hat{d}_i = 0 \tag{13}$$

$$p = \prod_{i=1}^{m} p_i = 1 \tag{14}$$

Shifting Branch (Pseudo Node)

To connect pins of gates working under different reference voltages, it is necessary to define a network element called *shifting branch* (Bezugspotentialschieber), that appears only in the delay scheme, not in the logical scheme of the same circuit. The shifting branch has an transition ratio of one, and causes a delay time τ proportional to the transition time T.



$$\tau = \mu/f = \mu T \tag{15}$$

$$p = f_a/f_e = 1 \tag{16}$$

In delay schemes node loads are shiftable over shifting branches.

5. DELAY MEASUREMENTS

To prove the applicability of the proposed delay rules, it is possible to investigate a simple gate in the full range of input slopes.

Figure 3 shows a circuit simulation of a 5 μm NAND6-gate with *input slopes varying from* 1 kHz *to* 1 GHz (source [6]). The input transitions are not drawn. In respect to Chapter 3 an exact measurement of gates is possible by choosing carefully the reference voltages to more than 4 digits behind the decimal point.

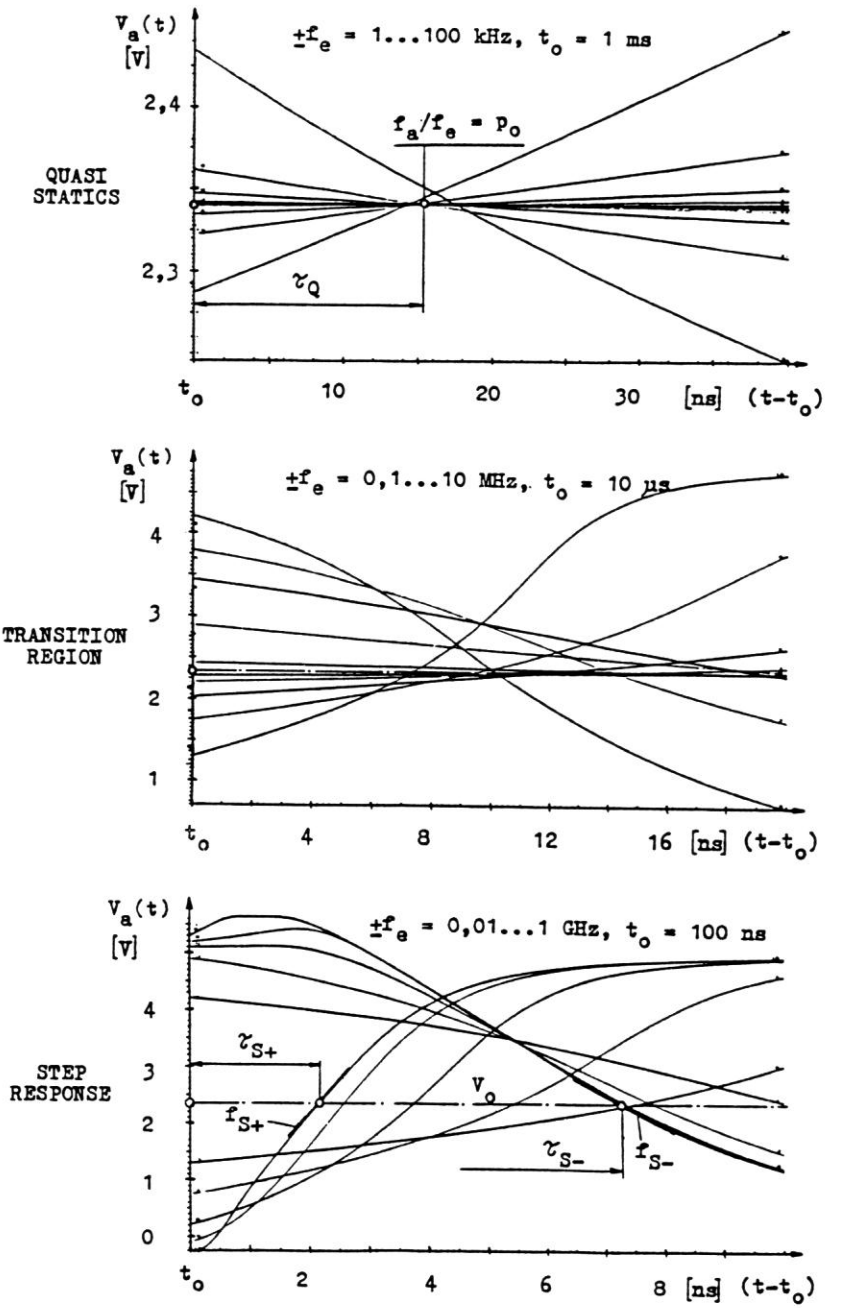


Figure 3 Circuit simulations at a NAND6. Output reactions under input slope variation f_e. Input edges are not drawn. The dashed lines mark the reference voltage. All input edges crosses the reference at t_0.

To find this reference voltages, a static circuit simulation of the short-circuited gate is necessary. In this case, proposed by *M/C* [2] in 1980, input and output get the same reference levels for $I_a = 0$. For practical use it is possible, to measure the reference voltages directly at test gates on the chip about multiplexing structures and opamps.

Figure 3 shows all output transitions (positive and negative) for input transitions increasing with a factor sqrt(10) = 3.162. . . It is of some interest, to see the *continuum between analog and digital circuit theory in one diagram.* The step responses show large timing differences between the transition times τ_{s+} and τ_{s-}. Pulling down the output for this six input CMOS-NAND is much harder, than pulling it up. As more one comes to quasi statics, than more the delays of

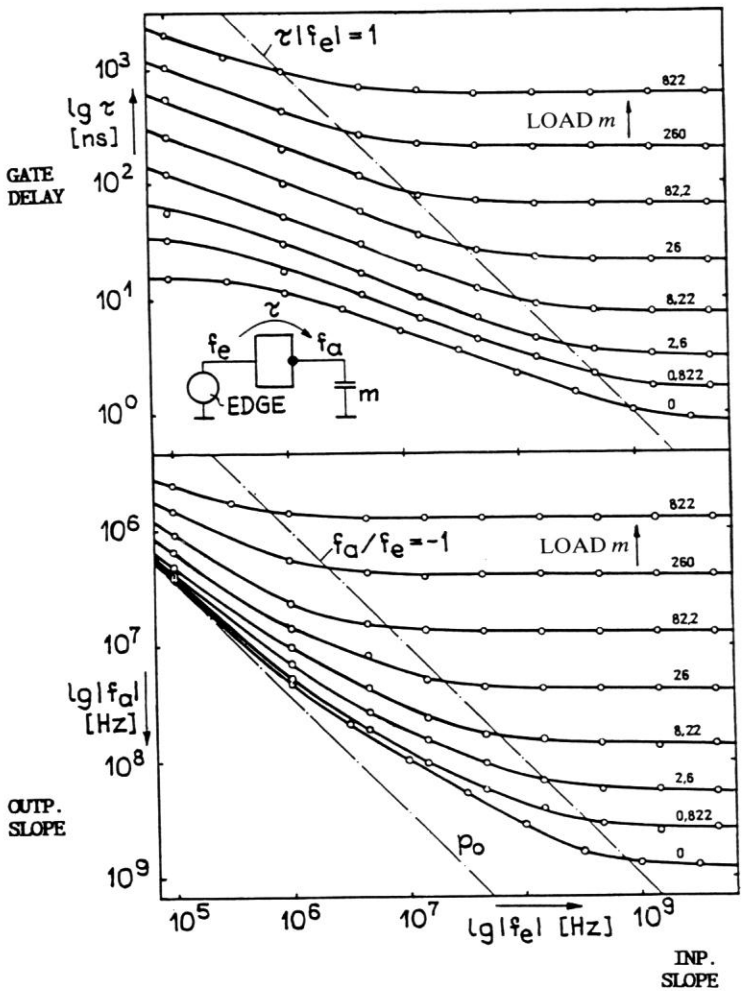


Figure 4 A dynamic transfer diagram of an inverter shows variations of the input slope f_e and the load factor m together.

both transition directions appear similar. The quasi static delay

$$\tau_Q = r_0 C_{\text{load}} \tag{17}$$

is *equal for both transition directions* and closes the bridge to the linear circuit theory. For further decrease of the input transition slope the quasi static delay τ_Q as like as the transition ratio $p_0 = f_a/f_e$ remains constant (source [6]).

To *examine the influence of load* onto the type of the transition region between quasi static an step response, Figure 4 shows a set of simulation results in a wide range of load factors $m = C_{\text{load}}/C_{\text{gate}}$. Medium was an 5 μm- inverter. For each load factor m the curves appear in an comparable form. They seem to be shiftable along the broken lines

$$\tau\,|f_e| = 1 \quad \text{and} \quad f_a/f_e = -1. \tag{18}$$

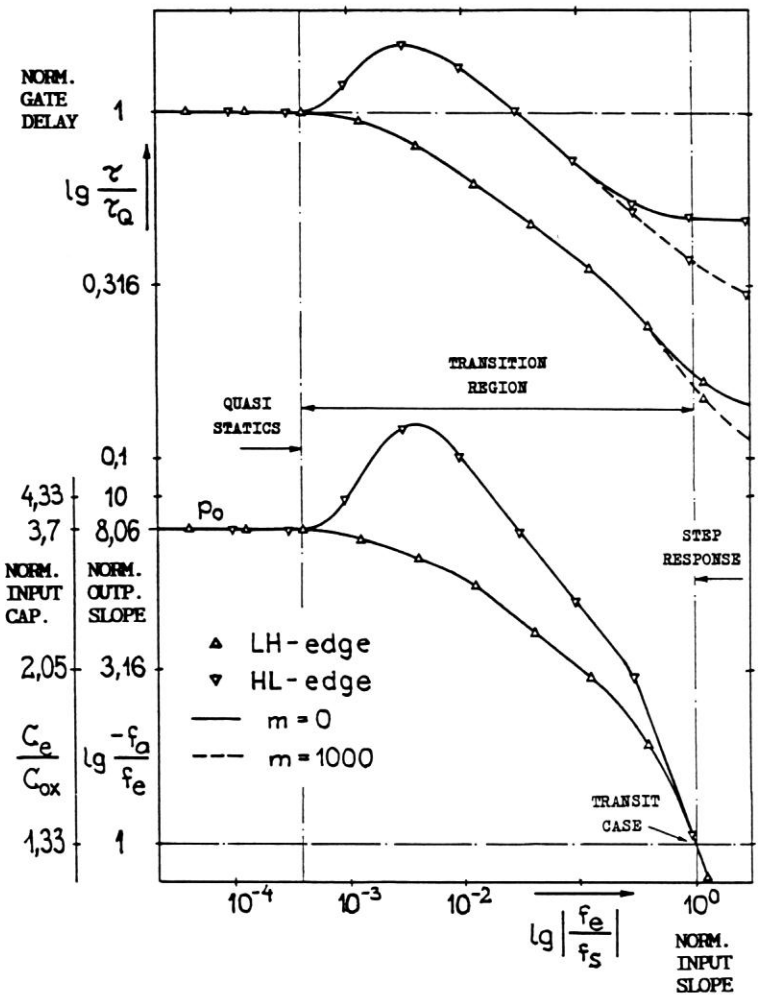


Figure 5 A normalized dynamic diagram (NAND6) includes all the dynamic relevant informations in a compact form.

Thus it seems possible to normalize every delay τ to the quasi static delay τ_Q under the same load; every output transition slope f_a to the input transition slope f_e; and the input transition slope f_e to the step response transition slope f_{Sx} under current load. x stands for the dependence on the transition direction. Figure 5 shows such a normalization. *Each input* (of one of the most asymmetric gates NAND6) *can easy be modelled by four simple curves for all possible loads.* For practical use it is sufficient, to model only one often used load factor. Then errors appear as delay reserves under increasing loads. Smaller loaded gates have absolute lower delays, hence a smaller error influence.

With increasing transition transfer ratio f_a/f_e the input capacitance C_e of the gate raises due to an increasing Miller effect within the transition time $T = 1/f_a$ of the output.

$$C_e = C_{ox}\left(1 - \frac{f_a}{f_e} k_m\right) \tag{19}$$

k_m is nearly a constant ($\approx 1/3$). C_{ox} is the oxide capacitance of the input transistors. Figure 5 shows, that C_e increases with high (negative) transfer ratios. C_e is neglectable in the uncritical region of step response. But if the gate has to drive a very small load, the input capacitance grows up to a more times higher value.

The dynamic simulations in Figures 3, 4 and 5 were done with a circuit simulator having a special written transition generator EDGE and an transition slope indicating unit OSZI. The input parameters for EDGE are low and high signal level, reference voltage, reference time and transition slope. It creates a continuous transition consisting of two sinus pieces connecting in (v_k, t_n). OSZI gets a reference voltage, and measures the time point for a crossing transition.

Which importance has a normalizeability of the dynamic behavior of gates on delay verifications?

Suppose, the correctness of drain current in a static transistor model is in some working areas not better than ±50%. Then any dynamic circuit simulation done with this model can produce nearly the same fault value. The normalized transfer characteristics (Figure 5) shows, that *dynamic measurements of gates can succeed under every possible t.m. very large load capacitances.* Thus, now it is possible, to measure the dynamics of a gate directly with hardware. If the value of the load and some static output currents are known (Figure 6), every digital verification with this direct model can nearly be as exact as a circuit simulation.

6. A TIMING VERIFICATION ALGORITHM

The knowledge about dynamic diagrams we can now use to construct the core of a short and precious timing verification algorithm. It has to compute one timestep calculation per transition, ever in straight forward or in iterative manner.

Independent of the hierarchical level a cell or a block has one and only one affecting transition and one corresponding input that causes a reaction at the output(s). Needless to say, that different actions mostly have different signaling sources. A block, having two or more affecting inputs simultaneous mostly

operates not well. The exact timing of such a race is unimportant. The designer only tries to avoid this condition. Thus crossing, overlapping transitions have to produce warning messages. The algorithm can not well calculate race conditions.

Parameter Description

Input and output pins of cells or blocks get pin and/or event located parameters.

pin_located
  reference_voltage
  node_capacitance (straight forward working)
event_located
  reference_time
  transition_slope
  node_capacitance (iterative working simulator)

Algorithm

Step response and quasi static response show relations between static and dynamic gate parameters. Delay τ_{Sx} and transition slope f_{Sx} for step response equates to a gate constant multiplied with the load C (details see [1]).

$$\tau_{Sx} = U_{Sx}C/(-I_{Sx}) + \tau_m = C \cdot k_{\tau x} + \tau_m \tag{20}$$

$$f_{Sx} = -I_{Sx}/(U_{\text{hub}}C) = 1/C \cdot k_{fx} \tag{21}$$

$k_{\tau x}$, τ_m and k_{fx} are static, gate dependent constants. Index x shows a transition direction dependency. It has two values ($\pm$). Figure 6 allows to deduce these equations.

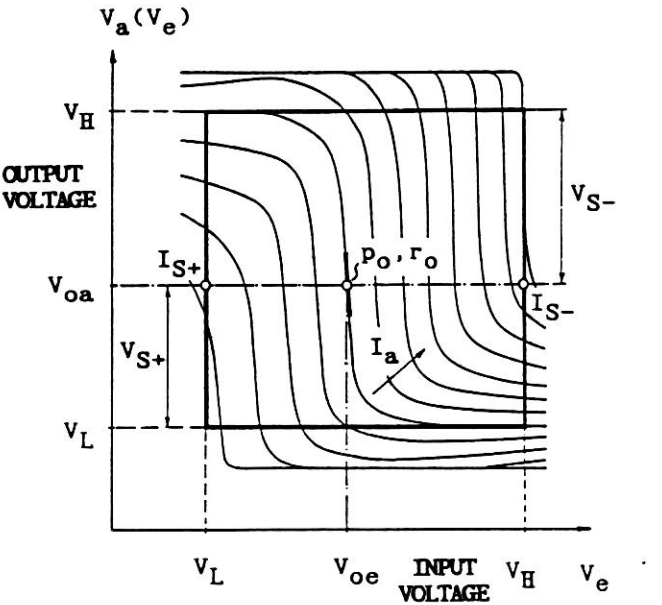
To reduce the influence of measurement faults the normalization of τ in practical approaches should be better to τ_{Sx} than to τ_Q (compare Figure 4). For each input of a gate we get a set of four curves, two delay and two transition transfer curves for each transition direction. To obtain a delay τ and an output transition slope f_a for a given input transition slope f_e from a normalized diagram, use the following algorithm.

Given are the inputs f_e, C_i and $k_{\tau x}$, τ_m, k_{fx} as gate parameters; Calculate τ and f_a (first we suppose C_e is constant):

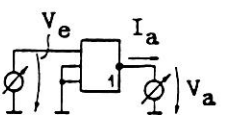
- Calculate the level-shift delay $\tau_\mu = \mu/f_{i-1}$ [1 sub, 1 div] {Equation 8}
- Calculate the sum of node loads, $C = \sum C_i$ [some adds]
- Calculate $1/f_{Sx}$ [1 mul] and τ_{Sx} [1 mul, 1 add] {Equations 20, 21}
- Calculate the ratio $f_e \cdot 1/f_{Sx}$ [1 mul]
- Diagram: look for the corresponding f_a/f_e and τ/τ_{Sx}
- Calculate $f_a = (f_a/f_e) \cdot f_e$ [1 mul]
- Calculate $\tau = (\tau/\tau_{Sx}) \cdot \tau_{Sx}$ [1 mul]
- Calculate the new reference time $t_i = t_{i-1} + \tau_\mu + \tau$ [some adds]

If C_e shall be a function $\{C_e = f(f_a/f_e)\}$ then add:

- Calculate new input capacitance C_e [1 add, 1 mul] {Equation 19} for the next iteration or call



$$I_{S+} = I_a(V_L,\ V_{oa}) \qquad I_{S-} = I_a(V_H,\ V_{oa})$$



$$p_o = \left.\frac{dV_a}{dV_e}\right|_{V_{oa},\ V_{oe}} \qquad r_o = \left.\frac{dV_a}{dI_a}\right|_{V_{oa},\ V_{oe}}$$

Figure 6 A static diagram with dynamic relevant static gate parameters.

A full implementation of this algorithm costs for the computation of one HL- or LH-transition passing through a gate some additions, six or seven multiplications and zero or one division.

Compared with well-known algorithms of comparable precision [9] this algorithm has a very low computational expense.

7. BINDING DYNAMICS TO STATICS

It seems to be of some interest, that ratios of dynamic parameters of the gate are joined with static parameters. For example, the ratio between the delays of quasi

statics τ_Q and step response τ_{Sx} is deduceable from static parameters (see [6]), Figure 6.

$$\frac{\tau_Q}{\tau_{Sx}} \approx \frac{r_0 |I_{Sx}|}{|U_{Sx}|} \tag{22}$$

Also the length of the transition region between quasi static and step response is defined. The step response of an AOI-gate begins nearly at the transit case (Transitfall) $f_{aT}/f_{eT} = -1$. The ratio $p_a = f_{aT}/f_{aQ}$ characterizes the transition length at the gate output. The ratio $p_e = f_{eT}/f_{eQ}$ characterizes the transition length at the gate input. Combining this equations together, a simple equation appears (source [6]).

$$p_a = p_e/(-p_0) \tag{23}$$

The length of the transition region at the output of the gate is p_0 times smaller, than the length of the transition region at the gate input (p_0 is the static gain dV_a/dV_e (mostly negative) of the AOI-gate at the reference voltages.

We know this phenomenon well. An AOI-chain, consisting of many gates, replies with nearly the same transition slope independent from the transition slope at the affecting input. For the i gates long AOI-chain with all gates having the static gain p_0 the wide of the output region p_a decreases with the ith root of p_0.

$$p_a = \frac{1}{-p_0}\left(\frac{1}{-p_0}\left(\cdots\left(\frac{1}{-p_0} p_e\right)\cdots\right)\right) \tag{24}$$

$$\frac{p_a}{p_e} = \frac{1}{-p_0^i} \tag{25}$$

8. CONCLUSION

A comprehensive look to reference voltages of digital transitions with finite transition slopes opens the view to some interesting, up to now unknown details. A Taylor expansion can show a transition as a triple of values {*reference time, reference voltage, transition slope*}. With this definition it is possible, to examine gates continuously between step response and quasi statics. Digital delays appear as vectors. Measurements of gates can be more exact, interface descriptions become easier, exact timing descriptions of block hierarchies as 'black boxes' will be possible. Delay rules permit the composition of delay schemes. Special reference voltages for $I_a = 0$ allow closed simulations from quasi static to step response: a relationship between the (nonlinear) digital and the (linear) analog circuit theory was shown. An examination of dynamic diagrams with varying input slopes and varying output loads shows Mead's 1980 predicted normalizeability [2] of gate dynamics. As example, a core of a timing verification algorithm is proposed using the new ideas. Final, some deductions are derived declaring well known peculiarities of AOI-gates.

Acknowledgments

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